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VLSI SOCIETY OF INDIA

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4th Workshop on Design Verification Methodologies

April 25-26, 2008

The Capitol Hotel, Rajbhavan Road, Opp GPO, Bangalore 560001

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<http://www.thecapitolhotel.com/>


Nanotechnologies have ushered in System-On-Chip designs with 50 million gates. Functional and timing verification of such designs is a formidable task. Design Verification has been known to be biggest contributor to the design cycle time. Statistics also indicate that design respins are often due to functional bugs detected late.

Cutting down the time for verification is one of the major goals of design teams across the globe. Many new methodologies have emerged towards solving this problem.

This two-day workshop is intended as a forum to discuss the new trends and methodologies for Design Verification.

It is also a forum to share current practices in Design Verification.

HISTORY:

The first workshop in this series was held on November 25, 2005 at Hotel Atria, Bangalore and was attended by about 60 professionals:

http://vlsi-india.org/vsi/activities/dvw05_blr/

The second workshop was held during March 24-25, 2006 at Wipro Technologies, Pune and was attended by about 60 professionals:

http://vlsi-india.org/vsi/activities/dvm06_pne/

The third workshop was held during April 5-6, 2007 at I Square IT (I2IT), Pune Campus, and was attended by about 75 participants:

<http://vlsi-india.org/vsi/activities/2007/dvm-pune-apr07/index.shtml>

The workshop is suitable for practitioners of Design Verification and for students/faculty who are engaged in VLSI design projects.

Speakers

Prabhat Agarwal, Sankalp Semiconductor

Aniruddha Baljekar, NXP Semiconductors

Ansuman Banerjee, Interra Systems India

Gurudutt Bansal, Cadence Design Systems

Vishal Choudhary, NXP Semiconductors

Pallab Dasgupta, IIT Kharagpur

Kaushik De, Synopsys India

Sainath Karlapalem, NXP Semiconductors

Raj Mitra, Texas Instruments India

Abhijit Ray, Cadence Design Systems

Badri Seshadri, NXP Semiconductors

Pradip Thaker, Analog Devices Inc.

Srinivasan Venkataraman, Synopsys India

Haridas Vilakathra, NXP Semiconductors

Registration: Registration form is provided at the end of this announcement.

Category	Before March 31, 2008	After March 31, 2008
Professionals (Non-Members)	Rs. 4,000/-	Rs. 4,500/-
Professionals (VSI/ IEEE members)	Rs. 3,000/-	Rs. 3,500/-
Students/ Faculty (Non-members)	Rs. 2,500/-	Rs. 3,000/-
Students/ Faculty (VSI/ IEEE members)	Rs. 2,000/-	Rs. 2,500/-

Please also register using the online registration form at <http://vlsi-india.org/vsi/activities/reg.shtml> apart from sending the filled hardcopy of registration form, and to notify spot-registration.

Program Schedule

... April 25 – Friday ...

08.00 – 09:00 AM	Registration
09:00 – 09.30 AM	Inauguration
09.30 – 10.30 AM	Session I Keynote Talk – Pallab Dasgupta , IIT Kharagpur Model-Driven Integration: Putting together the bits and pieces of verification
10.30 – 11.00 AM	Tea
11.00 – 12.00 PM	Session II Low power Verification Abhijit Ray , Cadence Design Systems
12.00 – 01.00 PM	Session III Holistic Verification: Myth or The Magic Bullet? Pradip Thaker , Analog Devices Inc.
01.00 – 02.00 PM	Lunch
02.00 – 03.00 PM	Session IV Need for methodology in Functional Verification Srinivasan Venkataramanan , Synopsys India
03.00 – 03.30 PM	Tea
03.30 – 04.30 PM	Session V Realizing Design for debug infrastructure in complex SoC Haridas Vilakathra , NXP Semiconductors
04.30 – 05:30 PM	Session VI Verification Re-Use in RTL and SystemC IP Aniruddha Baljekar , NXP Semiconductors
End of Day-1	

... April 26 – Saturday ...

09.00 – 09:30 AM	Registration
09.30 – 10.30 AM	Session I Keynote Talk – Kaushik De , Synopsys India Verification of Clock Domain Crossing in Today's Complex SOCs
10.30 – 11.00 AM	Tea
11.00 – 12.00 PM	Session II Coverage driven Verification Gurudutt Bansal , Cadence Design Systems
12.00 – 01.00 PM	Session III Verification Methodologies for Analog Design Modules/Blocks Prabhat Agarwal , Sankalp Semiconductor
01.00 – 02.00 PM	Lunch
02.00 – 03.00 PM	Session IV Increasing dynamic assertion-based verification productivity with formal techniques for compositional coverage analysis Ansuman Banerjee , Interra Systems India
03.00 – 03.30 PM	Tea
03.30 – 04.30 PM	Session V Systematic Approach for Verification of Complex SoC Badri Seshadri , Sainath Karlapalem , and Vishal Choudhary , NXP Semiconductors
04.30 – 6.00 PM	Panel Discussion: Verifying monster SOC - Whose job is it anyway? Moderator: Raj Mitra , Texas Instruments India Panelists: Ish Dham , Texas Instruments India; Pradip Thaker , Analog Devices Inc.; Gurudutt Bansal , Cadence Design Systems; Srinivasan Venkataramanan , Synopsys India; Giri Raju , Wipro Technologies; and Sundaresan Kumbakonam , Broadcom Issues to be addressed in the panel are the following: How and where should the verification job be partitioned? 1) IP vs SoC teams, 2) Design vs Verification teams, 3) Hardware vs Software teams, 4) Inhouse vs Outsourcing options Since the job does not wholly belong to one specific team, how is the responsibility and accountability tracked? That is, who gets the credit if the chip succeeds, who gets the blame if a respin occurs? What are the best practices that are followed for this partitioning and tracking? What are the areas of ambiguity and conflict? Are there any methodologies / technologies which can help to objectively answer these questions through measurable metrics? How does Formal verification influence the answers to these questions? How does mixed-signal further complicate the problem?
End of Workshop	

Day-1 (April 25, 2008)



Model-Driven Integration: Putting together the bits and pieces of verification

Dr. Pallab Dasgupta did his B.Tech, M.Tech and PhD in Computer Science from the Indian Institute of Technology Kharagpur. He is currently a Professor at the Dept. of Computer Sc. & Engg, I.I.T. Kharagpur. His research interests include Formal Verification, Artificial Intelligence and VLSI. He has over 80 research papers and 2 books in these areas. He currently leads the Verification group at the CSE Dept., IIT Kharagpur (<http://www.facweb.iitkgp.ernet.in/~pallab/forverif.html>) which has ongoing research collaborations with several companies, including Intel, Synopsys, General Motors, National Semiconductors, IBM and Google.

Dr Dasgupta has been a recipient of the Young Scientist awards from the Indian National Science Academy, Indian National Academy of Engineering, and the Indian Academy of Science. He is a senior member of IEEE. Since Oct '2007 he has been the Professor-in-charge of the Advanced VLSI Design Laboratory, IIT Kharagpur (<http://vlsi.iitkgp.ernet.in>)

Abstract:

As designs go multi-core, the task of verifying whether a set of pre-designed and pre-verified components are correctly integrated into the design is becoming a major challenge. Achieving meaningful simulation coverage over the integrated design is rapidly becoming infeasible under time-to-market constraints. The EDA community is faced with two broad options – (a) develop new tool suites that enable a correct-by-construction approach to design integration, and (b) raise the level of abstraction at which the integration is verified thereby providing more bandwidth for verification. Methods for functional coverage analysis and verification re-use are key requirements in both approaches. This talk will present an emerging approach towards top-down integration of the components of an integrated circuit, namely model-driven integration, and the corresponding verification problems. The talk will focus on the role of formal and semi-formal coverage analysis, abstractions, and their relation with simulation based approaches.



Low power Verification

Abhijit Ray is B.Tech in Electronics from BITS, Pilani and has over 8 years of experience in EDA product developments in the area of verification and a total of 16 years experience in product development and management. Currently he is working as R&D Director at Cadence NOIDA facility and managing the simulation R&D team.

Abstract:

Low-power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power consumption is as important as performance and area. As the importance of power grows in today's technologies, low-power verification takes a key role. It is now critical for the designers to implement power reduction methodologies at the architectural stage. The discussion will be around some of the power reduction techniques used today along with the possible problems associated with them.



Holistic Verification: Myth or The Magic Bullet?

Dr. Pradip Thaker has 15 years of industry experience combined both as a technical manager and individual contributor in developing large and complex ICs for networking, multi-media and computer connectivity with semiconductor and system companies in USA and India. He also served as an adjunct faculty at the George Washington University (Washington DC, USA) from years 1993-2003 where he designed and taught undergraduate and graduate level VLSI courses on part-time basis. He received BE (ECE), MS (EE) and PhD (VLSI Systems) in 1989, 1993 and 2000 respectively.

He is currently with DSP IC Division of Analog Devices, Inc. in Bangalore, India.

Dr. Pradip Thaker is recipient of industry and academic awards for excellence. He has published in international conferences and regularly reviews papers for the same. His technical contributions in industry are in the areas of architecture definition, RTL implementation, verification, synthesis and DFT. His academic research interests are in area of DFT and verification.

Abstract:

With advances in submicron technologies over last decade, multi-million gate ICs have become a cliché. With growth in size of the design, the diversity in functionality on a single-chip has proportionally grown while the time-to-market pressures have remained unchanged. On a single-die, it is common to have variety of combinations of newly developed digital as well as mixed-signal/analog circuits, integration of in-house and/or 3rd party IPs, integration of mega-blocks such as RAMs and ROMs, single or multiple instances of processor core(s), implementation of newly developed algorithms or standards with strict requirement for logical and electrical compliance, variety of standard and non-standard interfaces, integration of building blocks created through orthogonal design flows such as RTL and custom design. With convergence of these multiple disciplines on a single-die, verification of such IC is beyond the scope of any single verification approach. Even brute-force cumulative deployment of all verification techniques each of which is traditionally used to tackle a respective challenge is insufficient to produce high-quality robust first silicon. In this presentation, a holistic verification strategy will be defined and discussed with aim to provide guidelines for high-confidence verification sign-off of high-end multi-million gate devices with feature and flow diversities. Trade-offs of various emerging and incumbent verification techniques will be presented along with best practices from both, academics and industry.



Realizing Design for debug infrastructure in complex SoC

Haridas Vilakathra started his career as a scientist at DRDO (1994-1998) where he was involved in the development of hardware and software for a flight control system and airborne sonar. He later worked for NEC Japan (1998 - 2000) on hardware IP development, system integration and verification for a W-CDMA base station. He is presently with NXP semiconductors (2001-current) where his responsibilities include architecting of reusable hardware IP cores, processor based sub system and SoC validation. He has published more than 15 papers in national and international forums. His current interest is in defining a post silicon validation strategy for complex SoC, at hardware and system level.

Abstract:

Modern process technologies allow realization of large and complex hardware and software functions on a single chip. Because of these system complexities, improvements in hardware and software debug capabilities and IC verification techniques are necessary. In this talk we will discuss several industry wide approaches to address this problem, and outline the future directions in this regard. We then focus on the applicability of these approaches with a multi core SoC case study.



Need for methodology in Functional Verification

Srinivasan Venkataramanan is a Corporate Application Engineer (CAE) Manager with Synopsys, Bangalore - India. His areas of interest are the emerging verification solutions and methodologies such as SystemVerilog, VMM, Assertion-Based Verification, formal verification etc. He provides support to leading edge semiconductor design companies on their verification methodologies and challenges. In his previous employment with various design houses, he was actively involved in the verification of leading edge high-speed, multi-million gates ASIC designs. Srinu holds a Masters Degree from the prestigious Indian Institute of Technology (IIT), Delhi in VLSI Design, and Bachelors degree in Electrical engineering from TCE, Madurai. Srinu has co-authored the following books:

- A Pragmatic Approach to VMM Adoption
- Using PSL/Sugar, 2nd Edition and
- SystemVerilog Assertions Handbook.

Srinu has also presented in various conferences and forums such as DesignCon (East), DVCon, SNUG etc. Srinu has been delivering trainings on SVA, SVTB & VMM to Synopsys customers for 3+ years.

Abstract:

Functional Verification has been one of the biggest bottlenecks of an ASIC/SoC design project for several years now. Statistics show that the time it takes to put together a design is significantly less than it takes to make sure the design is functionally correct and usable. In other words, the ability to design has far exceeded the ability to verify the same. One of the main reasons why the "ability to design" has increased, is due to the industry wide adoption of sophisticated approaches to IP reuse on the design front. This dates back to the late 90s, when a definitive text on Design Reuse was published as a standard book named RMM (Reuse Methodology Manual). However, similar adoption has not been widespread on the verification side. Problem is not that DV teams don't know how to verify, rather it is the opposite: there are too many ways to achieve this and a common baseline has not been well accepted. This has resulted in a situation wherein ever DV team adopts ad-hoc approaches to perform similar tasks in verification resulting in non-reusable components, undocumented ideas etc. Unlike on the design side, the requirement of a methodology for Verification has not been well understood by a large section of the DV community. This has led to many diverse approaches to Verification, leaving the new users confused about the right way to approach the verification problem. More often than not engineers want just a handful of powerful language features and would rather build recipe on their own. While this is doable (and has been working), it is not as scalable as a methodical approach to verification. In this talk the author presents the needs for a standard methodology for design verification based on the de-facto industry standard, VMM for SystemVerilog.



Verification Re-Use in RTL and SystemC IP

Aniruddha Baljekar is working in the System and Software Design Environment (SSDE) group of NXP at Bangalore, India on Advanced Functional Verification (AFV) for the last 7 years. The group focuses on System Level Design methodologies, Software Design Technologies, Transaction Level Modeling. Currently he is working on the coverage driven verification methodology in verification of high level TLM models developed in SystemC.

Abstract:

With the complexity of the design components on the rise, coverage of functional verification is one of the increasing challenges faced by the design and the verification teams. Reducing the verification time without compromising the quality of the verification is the greatest challenge to the verification engineers. Improving the verification process is highly critical to improve on the time to market. To achieve this, re-use of the verification environment across different levels is the way forward. The re-use of the verification environment can be achieved at following levels: Reuse with different IPs, Reuse at different levels of integration and Reuse at different levels of abstraction (SystemC (PV/PVT), RTL)

The paper covers the following:

- Methodology adopted to address the reuse of the test environment/testbench at unit level across testing of highly abstract level models (modeled in SystemC) and RTL models (modeled in VHDL/Verilog)
- Methodology and challenges faced towards unit level verification of complex TLM (SystemC) model (memory controllers: external static memory controller and external nand flash controller) using this re-use methodology
- Methodology in creating verification IP's to provide interfaces to enable its re-use at these different levels of abstraction

Following tools are used in this methodology:

- Specman Elite as the functional verification tool, which supports coverage driven verification methodology
- vManager for plan driven verification
- Scenario builder to create specific scenarios
- eVCs as the verification IP's

Day-2 (April 26, 2008)



Verification of Clock Domain Crossing in Today's Complex SOCs

Kaushik De received B. Tech from IIT Kharagpur, and MS and PhD from University of Illinois at Urbana-Champaign. He worked in various technical & management roles in LSI Logic, Ambit, Cadence, Synopsys, and various startup companies, in US and India. He has worked in the area of Synthesis, DFT, and Design Verification. Currently he is R&D Director at Synopsys, working in Design Verification area, driving the static checker technology. He has published more than 20 technical papers at conferences and journals, and holds 5 US patents.

Abstract:

As capacity is growing, more and more functionality is put into a single chip. As a result today's SOCs contain many asynchronous clocks. Designing and verifying interaction between signals between asynchronous clock domains is major challenge, because signals crossing clock domains need to follow strict rules to ensure correct functionality. Many design re-spin happens due to bug in clock-domain crossing issues. In order to verify correctness of clock-domain crossing, comprehensive methodology needs to be followed encompassing structural, formal and simulation techniques. This talk will discuss the challenges and techniques in clock domain crossing verification.



Coverage driven Verification

Gurudutt Bansal is an Engineering Director in the Verification Division at Cadence Design Systems. He manages the R&D for Incisive Technologies with his main focus being Coverage Driven Verification solution and RTL Analysis. Gurudutt has 15 years of experience in the EDA industry, with over 10 years of experience in the Verification domain. This includes native HDL simulation, Coverage and Assertion-based verification technologies. He has a Bachelors degree in Computer Engineering from the Delhi Institute of Technology.

Abstract:

The primary purpose of Functional Verification is to identify the verification goals mapped to the specifications of the design, and execute this plan as per these defined goals. The key attributes of a verification methodology include

- Defining the verification goals and a verification plan
- Executing the plan
- Defining the metrics, which are typically Coverage metrics, to measure the progress of verification and quality of testing
- Automating the complete verification process

The talk will provide an overview of the Coverage Driven Verification (CDV) methodology from verification planning to closure. It will provide information on various Coverage metrics - code, assertion and functional, coverage data collection and its analysis, and how to use it to measure progress and achieve verification closure. It will also discuss some of the challenges in developing and using the CDV solutions.

Verification Methodologies for Analog Design Modules/Blocks

Prabhat Agarwal joined Philips Semiconductor after completing his graduation from National Institute of Technology, Surathkal. During his tenure Prabhat was responsible for developing some of the key IO design and layouts in 180nm, 130nm and 90 nm technologies. This included IEEE-1394, general purpose IO and I2C interfaces. Before joining Sankalp Semiconductor, Prabhat was part of the IO development team in Infineon Technologies. As part of Infineon, Prabhat was leading many high-speed IO architectures, including Low Voltage Differential Signaling (LVDS) and Analog Macros like Oscillators. Works were mainly in the technology nodes of 90nm and 65 nm CMOS.

Prabhat hold 3 international patents and one publication. His passion is to create one of the best training system that will drive many students to become not just knowledgeable, but be the "best in the world" in the Mixed Signal. In Sankalp, he is leading the Analog Design Wing, New Module Development. The team is working on some State-of-the-Art Design Analog blocks/Modules with clear focus on quality and cycle time.

Abstract:

The verification of Analog Design Modules/Blocks are becoming more and more challenging during design and post design phase with the shrinking technologies. This tutorial is an attempt to discuss on issues that a Analog designer or Analog verification engineer faces for developing a complex modules/blocks where the numbers of corner cases increases exponentially with the process, voltage and temperature variation along with a matrix of performance parameters to be designed for the blocks. Then a verification methodology for Analog Blocks/Modules is presented to overcome some of these issues.



Increasing dynamic assertion-based verification productivity with formal techniques for compositional coverage analysis

Ansuman Banerjee is presently working as a Principal Engineer in the verification group at Terra Systems. He has completed his post-graduate and doctoral dissertations in the area of formal and semi-formal verification from the Indian Institute of Technology, Kharagpur. He has about 20 publications in areas related to verification in national and international conferences (DAC, ICCAD, VLSI etc.) and journals (ACM TODAES, IEEE TCAD etc). He has served on the Technical Program Committee of DVCON 2008 and has been a reviewer of the international conference on VLSI Design and VLSI Design and Test Workshop (VDAT).

Abstract:

Capacity limitations continue to impede widespread adoption of formal property verification in the design validation flow of software and hardware systems. The more popular choice (at least in the hardware domain) has been dynamic property verification (DPV), which is a semi-formal approach where the formal properties are checked over simulation runs. DPV is highly scalable and can support a significantly richer specification language as compared to languages supported by formal property verification tools. Though the main limitations of DPV revolve around its dependence on the coverage of the relevant scenarios by simulation, there appears to be ample scope of addressing these issues through formal methods for coverage and consistency analysis. This talk will present some new methods and techniques in this direction that can aid DPV in becoming more effective in practice and more formal in nature. The talk will discuss some issues related to compositional verification with assertion reuse and specification-directed DPV that can facilitate faster convergence of the verification cycle in an effective manner.



Systematic Approach for Verification of Complex SoC

Badri Seshadri , Sainath Karlapalem and Vishal Choudhary, NXP Semiconductors

Badri Seshadri, is Senior Technical Lead in charge of verification of complex SoCs for the Multimedia application chips. He is working with Philips Semiconductors for the past 7 years in the area of System Level Modeling and Verification . His area of interests are Application media SoC Verification and Performance Benchmarking of Platforms. Badri has a,B.E.(Hons) in Electronics and communication from Madras University and M.Tech in Electronics from BITS, Pilani.

Sainath Karlapalem received M.Tech degree in Digital Systems and Communications from National Institute of Technology, Calicut. He joined Central Research Laboratory of BEL in 2000 and worked for one year in the area of low bit rate speech codecs. He then moved to Philips Research and worked as Senior Research Engineer in the area of multiprocessor architectures. Currently he is working as Senior Technical Leader in NXP Bangalore. His interests include Design Space Exploration of Multiprocessor Architectures, Verification of Multiprocessor SoCs.



Vishal Choudhary received his B.E. degree in electronics engineering from the S.G.G.S College of Engineering and Technology, Nanded, India, and the M.Tech. degree in VLSI design tools and technology from the Indian Institute of Technology, New Delhi, India. From June 1999 till Oct 2006, he worked as Research Scientist in the Group Digital Design and Test, Philips Research Labs in Eindhoven, the Netherlands. His research interests include dynamic power management for SoC, low power VLSI design, and reconfigurable computing architectures. Currently, he is working as an Senior Architect with NXP Semiconductors in Bangalore.

Abstract:

Today's feature-rich multimedia devices both in mobile and home domain require complex SoC designs to meet market demands for high performance at low cost and energy consumption. Consequently, the demands by the high-end applications are mostly met by Multi-processor SoC architectures. Verification of complex Multi-processor SoC (MpSoC) throws up different uplift for the challenges in the chip level verification arena. This presentation covers a systematic verification methodology to verify the complex multimedia chips. Approach includes efficient simulation-time reduction techniques, test bench infrastructure and re-usability across different chips. This presentation will also share the inter-connect/interoperability verification software for chip level verification.



