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VLSI Society of India

DFM 2008 - One-day Seminar on Design For Manufacturability and Reliability

July 7, 2008, Bangalore, India

Venue: The Capitol Hotel



Rajbhavan Road, Opp GPO, Bangalore 560001; Tel: 080-22281234, 2228, 1800; FAX: 080-2225 9922, 2225, 9933

Website: www.thecapitolhotel.com

Design for Manufacturability:

Design for Manufacturability (DFM) is a design approach that simultaneously considers all of the design goals such as functionality, area, power and performance as well as constraints such as optical patterning limitations including diffraction and etch. Manufacturing yield can be improved through design process. Incorporating design practices to improve manufacturing yield is more commonly known as design for manufacturability. Recently DFM has received a lot of attention due to sub-wavelength lithography. In this talk, we will explore photolithography trends and how they restrict designs, lithography simulation basics, resolution enhancement techniques and describe the process of yield improvement through better physical design as well as yield recovery through test oriented learning process. We will show how Physical Design Rules are derived and managed to improve yield.

Design for Reliability:

Design for Reliability is an exercise in exploiting and managing redundancy. Redundancy is nominally defined as having more resource than is minimally necessary. Design for Reliability includes understanding and modeling the errors that result from device aging process, calibrating those models and avoiding errors through static or dynamic adaptations. In this talk, we will explore these topics.

Targeted Audience:

Targeted audience is practicing engineers, students and academics. Some physical design knowledge is helpful but not necessary. The topics covered are listed below. Handout will include a list of references for further exploration of the topic.

Course conducted by:

Sandip Kundu, University of Massachusetts, Amherst



Sandip Kundu is Professor of Electrical and Computer Engineering at the University of Massachusetts, Amherst. Previously he was at Intel Corporation (till January 2005). Prior to joining Intel, he was a member of the research staff at the IBM T. J. Watson Research Laboratory (1988-1997). He has published over 100 papers, holds 12 patents and has given 18 tutorials in forums such as ICCAD, EDAC, DATE, ASP-DAC, ATS, ETW and ITC. Sandip has also been in numerous program committees including DAC, ICCAD, DATE and ICCD. He was the technical program chair for ICCD 2000, general chair in 2001. He was the general chair of VLSI conference in India in 2005. He is currently a Distinguished Visitor of IEEE Computer Society, fellow of IEEE and an Associate Editor of IEEE Transactions on VLSI. Previously, he was an associate editor of IEEE Transactions on Computers.

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Registration Fee

Before June 30, 2008		After June 30, 2008	
Professionals (Non- Members)	Rs.3, 000/-	Professionals (Non- Members)	Rs.3, 500/-
Professionals (VSI/ IEEE members)	Rs.2, 500/-	Professionals (VSI/ IEEE members)	Rs.3, 000/-
Students/Faculty (Non-members)	Rs.1, 500/-	Students/Faculty (Non-members)	Rs.2, 000/-
Students/Faculty (Members of VSI/ IEEE)	Rs.1, 000/-	Students/Faculty (Members of VSI/ IEEE)	Rs.1, 500/-

The registration fee includes registration material, softcopy of notes, lunch and refreshments.

Mode of Payment: Demand Draft, drawn in favor of “**VLSI Society of India**” payable at Bangalore.

Please also register using the online registration form at <http://vlsi-india.org/vsi/activities/reg.shtml> apart from sending the filled hardcopy of registration form.

Seats are limited. Spot-registration subject to availability at the after deadline rates against DD or Cash.

DFM2007 was conducted during July 27, 2007 at Kolkata, India

Design For Manufacturability and Reliability

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Duration: Full day

Target Audience: Practicing Engineers, Design Professionals, Students and Academics

Registration	8.30 AM – 9.30 AM
Tutorial	9.30 AM – 5.30 PM
Morning Coffee break	11.00 AM -11.30 AM
Lunch break	1.00 PM – 2.00 PM
Afternoon Coffee Break	3.30 PM – 4.00 PM

Topics:

1. **Introduction**
2. **Litho simulation basics**
 - 2.1. Fraunhofer Diffraction
 - 2.2. Optical simulation of photomasks
 - 2.3. Quantitative models and techniques
 - 2.4. Litho printability issues & results from aerial simulation
3. **DFM topics**
 - 3.1. CMP modeling
 - 3.2. Resist modeling
 - 3.3. Resolution Enhancement Techniques (RET)
 - 3.4. RET issues and limitations
4. **Physical Design rules development and layout optimization techniques**
5. **Manufacturing Defects and Traditional Yield Modeling**
 - 5.1. Particulate defects
 - 5.2. Large parametric excursion
6. **Defect Modeling**
 - 6.1. For critical yield (critical area calculation and optical proximity correction)
 - 6.2. For parametric yield (litho and resist simulation)
7. **Litho Based Yield Modeling**
8. **Yield Models (with and w/o redundancy)**
9. **Defect Tolerance Techniques**
 - 9.1. Architecture based techniques (memories, processors, PLAs etc)
 - 9.2. Circuit/layout hardening techniques
 - 9.3. Algorithm based tolerance
 - 9.4. Statistical methods
10. **Reliability Issues**
 - 10.1. Hot Carrier
 - 10.2. NBTI
 - 10.3. Thermal
 - 10.4. Electro-migration
 - 10.5. Gate oxide problems
 - 10.6. Testing for reliability problems
 - 10.7. Soft-error
11. **DFR analysis and improvement techniques**

