Fourth VTU-VSI-ISA Confluence Meeting

February 28, 2007

Main Auditorium, R.V. College of Engineering, Bangalore, India

Organized by the VLSI Society of India

Supported by:

R.V. College of Engineering, Rashtreeya Sikshana Samithi Trust
Mysore Road, Bangalore
India Semiconductor Association

Visvesvaraya Technological University, Belgaum
http://www.vtu.ac.in/

VLSI Society of India
http://vlsi-india.org/vsi/

India Semiconductor Association
http://www.isaonline.org/

A forum for faculty, students, and the semiconductor industry.

The Indian Semiconductor Association (ISA), the Visvesvaraya Technical University (VTU), and the VLSI Society of India (VSI) jointly entered a Memorandum of Agreement (MoU) starting June 2005 with the goal of strengthening the industry-academia interaction.

The VTU-VSI-ISA confluence meeting provides a forum for faculty, students, and the semiconductor industry to come together. A memorandum of understanding was signed in August 2005 between the Visvesvaraya Technological University, the VLSI Society of India, and the India Semiconductor Association.

The intention of the MoU is to strengthen the bonds between VTU and the semiconductor industries in India. VTU represents a conglomeration of over 250 engineering colleges and gives the semiconductor industry a great opportunity to get involved with the academia, provide inputs in improving the curriculum, delivering seminars, teaching courses, and so on. The following colleges have been identified under this MoU to engage in academia-industry interaction, based on the M.Tech programs they have in microelectronics or allied areas:

- **BMS College of Engineering, Bangalore**
- **BVB Engineering College, Hubli**
- **VTU, Belgaum**
- **SJCE, Mysore**
- **UTL Extension Centre, Bangalore**
- **KLE, Belgaum**
- **RV College of Engineering, Bangalore**

Several meaningful meetings have been held among faculty champions and industrial representatives to give shape to the activities under the MoU.

June 27, 2005	VTU, VSI and ISA sign an MoU
February 24, 2006	First VTU-VSI-ISA Confluence meeting held at Bangalore
April 28, 2006	Second Confluence meeting held at Jnana Sangama Campus, VTU, Belgaum, Karnataka
October 30, 2006	Third Confluence meeting held at BVB College of Engineering, Hubli, Karnataka

The event on February 28, 2007 is the fourth of the major events that is being planned under the MoU. The intention of this meeting is to provide exposure of the happenings in the semiconductor industry to the M.Tech students of the participating colleges. Your active participation and constructive feedback on this event as well as the other activities of the MoU will be highly appreciated.

Visit http://vlsi-india.org/vsi/pub/confluence_24feb06.shtml for details on past confluence meetings.

Contact: Prof. Sarangapani Jagannathan Iyengar, RVCE (**jaggushar@rediffmail.com**)

Program Committee	Organizing Committee
C.P. Ravikumar, Texas Instruments, India	Prof. K. Balaveera Reddy (Patron)
Nagavolu Murty, NXP Semiconductors, India	Prof. Sarangapani Jagannathan Iyengar, RVCE
H.V. Ananda, Synplicity	Prof. K. Jayaraman, VTU
Manav Subodh, Intel India	Ms. Poornima Shenoy, ISA
Mahant-Shetti, KarMic, Manipal	Prof. V. Sreedhar, VTU
	Mr. S.R. Gopal Naidu, VSI
	Mr. Sunil Naidu, ISA
	Mr. Siddharth, RVCE
	Ms. B.V. Uma, RVCE

Registration: Refer registration form

VSI & IEEE Members: Students/ Faculty	Rs.500.00	**Non-Members: Students/ Faculty**	Rs.750.00	**Industry Participants**	Rs.1000.00

If you are not from VTU - Please also register using the online registration form at http://vlsi-india.org/vsi/activities/reg.shtml apart from sending the filled hardcopy of registration form, and to notify spot-registration.
If you are from VTU - Fellowships are available for students of VTU. Please contact Dr. Sarangapani Jagannathan Iyengar of RVCE (jaggushar@rediffmail.com) with details of your student/faculty status, year of graduation, program (M.Tech/B.Tech etc) before Feb 20.
All colleges that come under the VTU purview mentioned above.

Program Schedule

08.00 – 09:00 AM	**Registration**
09:00 – 09.30 AM	**Inauguration**
09.30 – 10.15 AM	**Session I** **The Challenges of Design for Manufacturability (DFM)** Anuradha Srinivasan, Intel India Chair: TBA
10.15 – 10.45 AM	**Tea**
10.45 – 11.30 AM	**Session II** **Multiprocessor Architectures for Embedded System-on-Chip Applications** **Dr. C.P. Ravikumar**, Texas Instruments India Chair: TBA
11:30 – 12.15 PM	**Session III** **Synthesis of Digital systems** Madhav Chikodikar, Synplicity Chair: TBA
12.15 – 01:00 PM	**Session IV** **High-speed Chip-to-chip Interfaces** Nisha P.K., Texas Instruments, India Chair: TBA
01.00 – 02.00 PM	**Lunch**
02.00 – 02.45 PM	**Session V** **Handheld Digital Video Broadcasting and Mobile T V** Arun Pradeep, NXP Semiconductors India Chair: TBA
02.45 – 3.30 PM	**Session VI** **Timing Analysis techniques in FPGA** Razak Mohammed Ali, Altera Semiconductor India Chair: TBA
03.30 – 04.00 PM	**Tea**
04.00 – 5.30 PM	**Panel Discussion** **"A Profession in Semiconductor Industry – What "IT" is and what "IT" is not"** Panelists will discuss what are the right expectations that students must have from the Indian semiconductor industry. **Moderator** – C.P. Ravikumar, Texas Instruments India **Panelists**: N.S. Murty, NXP Semiconductors India; A. Vasudevan, Wipro Technologies; Ram Jonnavithula, Texas Instruments India; V. Veerappan, Tessolve India
	Award Presentations, Announcements, and Conclusion

RV College of Engineering is located on Mysore Road. It is about 1 hr by road from the Bangalore Railway Station. Please check the Internet for directions, etc. For accommodation in Bangalore, you must check appropriate websites and make your own reservation. The organizers will not be able to provide accommodation.

Speakers brief-bio and abstract:

Anuradha Srinivasan completed BE (Electrical and Electronics) from BMS College of Engineering, Bangalore. She has 18 years of experience in VLSI, and has been with Intel for 4.5 years as Engineering manager. Currently, she is a member of Technical Staff in MGI. Prior to this, she was with National Semiconductors for 6.5 yrs and worked on technologies from 1 micron to 65nm and primarily in the backend area (Synthesis, STA, Physical Design).

The Challenges of Design for Manufacturability (DFM)
Abstract:
The presentation will provide an introduction to DFM and also talk about the challenges and changes to methodologies that this is bringing about for nanometer technology nodes.

C.P. Ravikumar is a senior technologist at TI India. He is also the secretary of the VLSI Society of India since 2003. More details about him can be found at http://cpravikumar.tripod.com

Multiprocessor Architectures for Embedded System-on-Chip Applications

Madhav Chikodikar is a senior manager for software development at Synplicity, Bangalore. He has around 12 years of experience in logic synthesis for ASIC/FPGAs, timing analysis and HDL front-end development. Prior to this, he was the lead developer with Synplicity, USA for their ASIC synthesis tool. Madhav also worked with SASKEN (formerly Silicon Automation Systems) on various projects in synthesis and HDL front-end development.

Synthesis of Digital systems
Abstract:
This presentation will cover different steps involved in mapping digital designs described at RTL level in HDLs such as Verilog or VHDL to ASICs and FPGAs. The presentation will briefly touch upon topics such as logic inference, module generation, two level and multi-level optimizations, technology mapping, timing analysis and timing optimizations. The presentation will also talk about the differences in mapping to FPGAs and ASICs.

Nisha PK graduated with a B.Tech in Electronics and Communication from Government Engineering College, Thrissur in 1998. She joined Texas Instruments, India, in 1999 where she has worked on design of telecommunication related IP, embedded memories, delay lock loops and Double Data Rate memories and interfaces.

High-speed Chip-to-chip Interfaces
Abstract:
As electronic equipment system-speed are increasing it is getting increasingly tougher to develop chip-to-chip data-transfer schemes, which can work reliably at high-speeds, in-spite of higher levels of noise jitter and signal integrity issues. In this presentation, we discuss various methods for chip-to-chip data exchange. These include schemes where the data is captured using the clock provided by the transmitter chip (source synchronous system), or schemes using a clock provided by the receiving chip (a non-source-synchronous system), or schemes using a clock provided externally to both transmit and receive, or a system where clock is recovered from the transmitted data. We also present the common concepts applicable to most of these schemes like jitter, ISI, SSO and other sources of noise, eye diagrams, link-timing budgets etc.

Arun Pradeep has Bachelor of Engineering [B.E] in Electronics and Communication and Master of Technology [M.Tech.] in Industrial Electronics. He has over 7.5 years experience in the IT industry. His Domain Experiences include Signal processing and embedded systems; audio, video and Imaging solutions for Digital TV, DVD and Mobile phones; short range communication systems [NFC] and navigation systems [GPS and DGPS]; identification systems for smart cards which includes Biometrics; Infotainment solution for car.

Handheld Digital Video Broadcast and Mobile T V
Abstract: The talk will mainly focus on advent of new mobile technology "TV on Mobile". Concepts of Digital video broadcast will be covered and extension of DVB to handhelds will be explained. Focus will be on architecture, design consideration and software stack. Finally cost models and billing models of consumer and service providers will be covered.

Razak Mohmmad Ali has worked for more than six years at Altera Semiconductor India, and is a University Program Manager looking after South-East Asia Pacific region. He obtained his MS from Texas, Austin; M.Sc. from IIT Khargpur, and MBA from Santa Clara University, USA.

Timing Analysis techniques in FPGAs
Abstract:
In this presentation we will investigate various techniques used in timing analysis of digital circuits implemented in FPGAs. Techniques for timing optimization and timing closure will be discussed. We will also briefly discuss how to incorporate Synopys Design Constraint (SDC) into FPGA design flow using the Timequest tool.

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REGISTRATION FORM

Name of the participant:

(Please use block letters.)

Category: Tick appropriate	Professionals (Non-VSI)		Member of:	Membership No:
	Professionals (VSI/ IEEE members)		VSI/ IEEE Membership No:	
	Students/ Faculty (Non-VSI)		Member of:	Membership No:
	Students/ Faculty (VSI/ IEEE members)		VSI/ IEEE Membership No:	

If you are a student, mention Semester/Year:

Contact Address: (Provide permanent mailing address)	**Designation:** Student Faculty Industry Other	
	College/ Company:	**Graduate by:** For students
	Department:	**Student ID:**
	Permanent address:	
E-mail: (Compulsory)		

Details of DD enclosed	Amount		DD Number	
	Drawn on Bank		Dated	

Mail the completed registration form and DD to the following address:

Mr. Gopal Naidu
Treasurer, VLSI Society of India
Finance Department
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park
C.V. Raman Nagar, Bangalore 560093

Please do not send scanned copies of DD by mail. Enter the payment details in the online form. An acknowledgement will be sent on receiving the regn.

- The DD to be made out to "**VLSI Society of India**" payable at **Bangalore**.
- On the back of the DD, please specify "**VTU-VSI-ISA Confluence - Bangalore**".
- Partial registration is not permitted. Processing fee of Rs.300/= will be charged against cancellation.
- Queries may please be sent to: vsisecy@vlsi-india.org
- Registration can be transferred to a colleague if intimation is provided 15 days before the event. (Provide the name in Capital letters)
- Spot-registration by cash or DD only.

Note:	Course fee includes registration material, lunch and refreshments. Transport and stay arrangements are the responsibility of the participants. **Please also register using the online registration form at** http://vlsi-india.org/vsi/activities/reg.shtml **apart from sending the filled hardcopy of registration form.**

This registration form is only applicable to non-VTU students/faculty. Fellowships are available for VSI students and faculty and they can be availed by writing to Dr Jagannathan of RVCE (jaggushar@rediffmail.com) Please include:

a. Your full name
b. Contract address
c. E-mail
d. College and Department
e. Student ID: (must be produced at the time of registration)
f. Will graduate by: (must be a student at the time of the event)