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Organized by



<http://vlsi-india.org/vsi>
VLSI Society of India

Two-day Course on Low-power Design and Test

July 30-31, 2007, Hyderabad, India
Venue: Hotel Green Park, Hyderabad

In cooperation with



C-DAC Hyderabad
and
VSI Chapter, Hyderabad

Greenlands, Begumpet, Hyderabad, Tel: 091 - 040 - 66515151, 23757575. <http://www.hotelgreenpark.com/hyderabad/index.htm>

Summary:

Power consumption of a CMOS circuit has emerged as an important design dimension in the nanometer era. The benefits of higher device density and increased clock rates for the modern VLSI system-on-chip (SOC) come at the cost of significantly increased power dissipation. Most VLSI devices and systems must consider low-power design and power management techniques. Requirements are driven by trends including the need to lower system costs (packaging/cooling), longer battery lifetimes for battery operated embedded systems, and often conflicting speed and power requirements.

This course provides an introduction to low power design and optimization techniques that would enable designers to build the ultra low power circuits of tomorrow. The instructors will draw from their experience in academia and industry to provide the necessary understanding of sources of power consumption in a CMOS circuit, power estimation techniques at various levels of design abstraction that provide an upfront opportunity to identify design hotspots, architectural and device-level power optimization and management techniques for designing a low power SOC, and power issues specific to manufacturing test that impact a modern chip design.

Targeted Audience:

The course is relevant to chip designers, low power EDA tool developers, academics and researchers working in the area of VLSI design. The topics covered are listed below.

Course conducted by:

Dr. Vishwani Agrawal, Auburn University, USA and **Dr. Srivaths Ravi**, Texas Instruments India



Vishwani D. Agrawal is James J. Danaher Professor of Electrical & Computer Engineering at Auburn University, Auburn, Alabama, USA. He has over thirty years of industry and university experience, working at Bell Labs, Rutgers University, TRW, IIT in Delhi, EG&G, and ATI. His areas of research include VLSI testing, low-power design, and microwave antennas. He has published over 250 papers, holds thirteen U.S. patents and has co-authored 5 books including Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits with Michael Bushnell at Rutgers. He is the founder and Editor-in-Chief of the Journal of Electronic Testing: Theory and Applications, was a past Editor-in-Chief of the IEEE Design & Test of Computers magazine, and is the Founder and Consulting Editor of the Frontiers in Electronic Testing Book Series.

Dr. Agrawal is a co-founder of the International Conference on VLSI Design, and the International Workshops on VLSI Design and Test, held annually in India. He served on the Board of Governors of the IEEE Computer Society in 1989 and 1990, and, in 1994, chaired the Fellow Selection Committee of that Society. He has received seven Best Paper Awards, the Harry H. Goode Memorial Award of the IEEE Computer Society, and the Distinguished Alumnus Award of the University of Illinois at Urbana-Champaign.

Dr. Agrawal is a Fellow of the IETE-India, a Fellow of the IEEE and a Fellow of the ACM. He has served on the advisory boards of the ECE Departments at University of Illinois, New Jersey Institute of Technology, and the City College of the City University of New York.



Srivaths Ravi received the B. Tech degree in Electrical and Electronics engineering from the Indian Institute of Technology, Madras, India and the M.A. and Ph.D. degrees in Electrical Engineering from Princeton University. At present, he is with the DSPS systems group in Texas Instruments, India. Previously, he was a research staff member with NEC Laboratories America, Inc, where he was responsible for developing RTL and C-based power estimation engines in NEC's C-based design flow. He also held a visiting research collaborator position with the Department of Electrical Engineering at Princeton University.

Dr. Ravi has worked in various areas including advanced embedded processing architectures, system-level and RTL test technologies, and low-power design. He has over 60 publications in leading ACM/IEEE conferences and journals on VLSI/CAD, including several invited contributions and talks. His papers have received awards at the VLSI design conference in 1998, 2000 and 2003, and the CODES/ISSS conference in 2006. He received the Siemens Medal from the Indian Institute of Technology, Madras, India in 1996. He serves in the organizing/program committees of various conferences including VLSI Test Symposium (VTS) and Design Automation and Test in Europe (DATE). He is a senior member of IEEE.

Registration Fee

Before July 21, 2007		After July 21, 2007	
Professionals (Non- Members)	Rs.4,000/-	Professionals (Non- Members)	Rs.4,500/-
Professionals (VSI/ IEEE members)	Rs.3,000/-	Professionals (VSI/ IEEE members)	Rs.3,500/-
Students/Faculty (Non-members)	Rs.2,000/-	Students/Faculty (Non-members)	Rs.2,500/-
Students/Faculty (Members of VSI/ IEEE)	Rs.1,500/-	Students/Faculty (Members of VSI/ IEEE)	Rs.2,000/-

The registration fee includes registration material, softcopy of notes, lunch and refreshments.

Mode of Payment: Demand Draft, drawn in favor of "VLSI Society of India" payable at Bangalore.

Please also register using the online registration form at <http://vlsi-india.org/vsi/activities/reg.shtml> apart from sending the filled hardcopy of registration form.

Spot-registration subject to availability at the after deadline rates against DD or Cash.

Program Committee:

Dr. C.P.Ravikumar, Texas Instruments India, **Dr. N. Sarat Chandra Babu**, CDAC, Hyderabad

Organizing committee:

Mr. M.V.Nageswara Rao, **Mr. Mahesh**, CDAC – Hyderabad; **Prof. C.D. Naidu**, HOD, ECE Dept, VNRVJiet, Hyderabad

Two-day Course on Low-power Design and Test

Duration: Two days. 9.00 AM to 5.30 PM

Registration on Day-1	8.30 AM – 9.00 AM
Course on all days	9.00 AM – 5.30 PM

Target Audience: Practicing Engineers, Design Professionals, Students and Academics

Schedule:

Day 1	09.00 – 10:30AM	Introduction	Vishwani Agrawal
	10:30 – 11.00AM	<i>Coffee break</i>	
	11.00 – 12:30PM	Dynamic and static power in CMOS	Vishwani Agrawal
	12:30 – 02.00PM	<i>Lunch</i>	
	02.00 – 03:30PM	Logic-level power estimation	Srivaths Ravi
	03:30 – 04.00PM	<i>Coffee break</i>	
	04.00 – 05:30PM	High-level power estimation	Srivaths Ravi
	Day 2	09.00 – 10:30AM	Architectural techniques: State machines, bus encoding
10:30 – 11.00AM		<i>Coffee break</i>	
11.00 – 12:30PM		Memory, multicore design	Vishwani Agrawal
12:30 – 02.00PM		<i>Lunch</i>	
02.00 – 03:30PM		High-level design methods Power management techniques	Srivaths Ravi
03:30 – 04.00PM		<i>Coffee break</i>	
04.00 – 05:30PM		Test power	Srivaths Ravi

