Updated December 11, 2007

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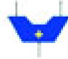

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Second International Workshop on Interconnect Design and Variability

December 13-14, 2007, Bangalore, India

Venue: "Room Conclave" **- The Atria Hotel**
P.B. No. 5089, No. 1, Palace Road, Bangalore - 560001
Ph: 91-080-22205205; Fax: 91-080-22256850
E-mail: atriahotel@yahoo.com, atriahotel@rediffmail.com
www.atriahotel.com

General Co-Chairs:

Nagaraj, N.S. Texas Instruments Inc., Dallas
C.P. Ravikumar, Texas Instruments India

Speakers:

Juan C. Rey, Mentor Graphics Corporation
Srinivas Mandavilli, Mentor Graphics India
Kazuya Masu, Tokyo Institute of Technology
Ersed Ackasu, OEA International, Inc.
Noel Menezes, Intel Corporation
Sachin Sapatnekar, University of Minnesota
Tom Williams, Synopsys
Vish Sundararaman, Texas Instruments Inc., Dallas
Steffen Rochel, Blaze DFM Inc.,
Nishath Verghese and **Atul Sharan**, Cadence Design Sys.
Nagaraj N.S. Texas Instruments Inc., Dallas
Palkesh Jain and **Gautam Kapila**, Texas Instruments India
Madhav P. Desai, IIT Bombay
Vani Prasad, Freescale Semiconductor India
Vidyasagar Ganesan, AMD

Workshop history:

The First IDV Workshop 2006 was held at IISc, Bangalore, during December 28-29, and was attended by 70 participants.
http://vlsi-india.org/vsi/activities/idv_dec06_blr/index.shtml

Scope of the Workshop

Interconnect scaling and variability are two difficult challenges in sub-100nm technology nodes. This workshop aims at addressing the following topics.

Latest advances in interconnect modeling and design innovations to continue performance scaling in sub-100nm technologies:

- Technology scaling trends
- New process realities in sub-100nm technologies
- Alternative interconnect methods
- Interconnect analysis algorithms
- Design and Architecture methods to mitigate RC scaling

In depth review of the latest advances in variability in sub-100nm technologies:

- Device and interconnect process variations
- Algorithms related to statistical analysis of performance and leakage
- Practical approaches to address variability
- Variation tolerant design methods

Targeted Audience:

The workshop will be useful to professionals as well as faculty and students who are looking for research topics.

Course Fee	Before November 30, 2007	After November 30, 2007
Professionals (Non-members)	**Rs. 5,000**	**Rs. 5,500**
Professionals (VSI/ IEEE members)	**Rs. 4,000**	**Rs. 4,500**
Students/Faculty (Non-members)	**Rs. 3,500**	**Rs. 4,000**
Students/Faculty (VSI/ IEEE members)	**Rs. 3,000**	**Rs. 3,500**

Please also register online at http://vlsi-india.org/vsi/activities/reg.shtml apart from sending the filled hardcopy of registration form.

Day-1 – Thursday, December 13, 2007

Interconnect RC parameters are significant components of circuit performance, signal integrity and reliability in IC design. Due to manufacturability and reliability issues, the effective dielectric constant of the inter-metal dielectric is not scaling commensurate with the technology scaling predicted in the ITRS roadmap. Metal resistance is also increasing due to electron scattering effects, which exacerbates the interconnect RC scaling issues in sub-100nm technology nodes. The increase in contact and via resistance further aggravates the technology entitlement issues. Although reverse scaling is an attractive option for high performance designs, area entitlement is an issue in routing limited designs. Overall improvement in interconnect performance relies more and more on architecture & design techniques and novel interconnect schemes. The sessions on Day 1 review interconnect scaling, signal integrity, physical design, architecture solutions and optical interconnect.

Schedule

Time	Session
08.00 - 08:30 AM	Registration
08:30 - 09:00 AM	**Inauguration** **Interconnect Design and Variability in Nanometer Era** **Nagaraj NS** and **CP Ravikumar**
09:00 - 10:00 AM	**Big Challenges for the Semiconductor Industry: Bridging Design and Manufacturing** **Juan C. Rey**, Mentor Graphics Corporation, **Srinivas Mandavilli**, Mentor Graphics India **Chair:** N.S.Nagaraj, Texas Instruments Inc., Dallas
10:00 - 10:15 AM	Break
10:15 - 11:15 AM	**On-Chip Global Interconnect Using Transmission Line** **Kazuya Masu**, Tokyo Institute of Technology **Chair:** N.S.Nagaraj, Texas Instruments Inc., Dallas
11:15 - 12:15 PM	**Interconnect Parasitic RLC and delay Variability below 90nm, Physical Origins and its Impact on the Future Geometry Scaling** **Ersed Ackasu**, OEA International, Inc. **Chair:** N.S.Nagaraj, Texas Instruments Inc., Dallas
12:15 - 01:00 PM	Lunch
01:00 - 02:00 PM	**Interconnect variability - A front-end perspective** **Noel Menezes**, Intel Corporation **Chair:** Shabbir Batterywala, Synopsys India
02:00 - 03:00 PM	**Thermal Challenges In Integrated Circuit Design** **Sachin Sapatnekar**, University of Minnesota **Chair:** Shabbir Batterywala, Synopsys India
03:00 - 03:15 PM	Break
03:15 - 04:15 PM	**Quality Now Requires - Small Delay Fault Model** **Tom Williams**, Synopsys Inc **Chair:** C.P.Ravikumar, Texas Instruments India
04:15 - 05:30 PM	**Panel Discussion: Managing Variability - should it be a Design Issue or a Test Issue?** **Participants:** Kazuya Masu, Ersed Ackasu, Noel Menezes, Sachin Sapatnekar, Tom Williams, Nagaraj N.S. **Chair:** C.P. Ravikumar, Texas Instruments India

Day-2 – Friday, December 14, 2007

Design For Manufacturability Yield (DFM&Y) has received much attention in sub-100nm technologies. Addressing the challenges in systematic and random process variations is a critical part of the DFM&Y strategy. Global and local variations in transistors have been analyzed in analog circuits for several years and recently extended to large-scale digital circuits in the form of Statistical Static Timing Analysis (SSTA). In additional to random variations, systematic variations such as stress induced variations need to be considered. In addition to transistor variations, interconnect variations due to Chemical Mechanical Polishing (CMP), etch and process bias are important considerations. Structured layout, variation-aware and variation tolerant design techniques help mitigate variability issues. The sessions on Day 2 review key aspects of lithography, CMP, etch and stress induced variations, SSTA methods and variation tolerant design techniques.

Schedule

08.00 - 08:30 AM	Registration
08:30 - 09:30 AM	**Process-aware Timing and Power Analysis and Optimization** **Steffen Rochel**, Blaze DFM Inc., **Chair:** Vivek Raghavan, Magma Design Corporation
09:30 - 10:30 AM	**Addressing pattern-dependent variability in design using model-based DFM tools** **Nishath Verghese** and **Atul Sharan**, Cadence Design Systems **Chair:** Vivek Raghavan, Magma Design Corporation
10:30 - 10:45 AM	Break
10:45 - 11:45 AM	**Design-In-Reliability for Interconnect** **Nagaraj N.S.**, Texas Instruments Inc., Dallas, **Palkesh Jain** and **Gautam Kapila** TI India **Chair:** Venugopal Puvvada, Quallcomm India Inc.
11:45 - 12:45 PM	**On the use of standardized interconnect in VLSI Systems** **Madhav P. Desai**, IIT Bombay and **Vani Prasad**, Freescale Semiconductor **Chair:** Venugopal Puvvada, Quallcomm India Inc.
12:45 - 02:00 PM	Lunch
02:00 - 03:00 PM	**Clocking in GHz designs** **Vidyasagar Ganesan**, AMD **Chair:** Vish Visvanathan, Texas Instruments India
03:00 - 04:00 PM	**Interconnect Design – Packaging Perspectives and Considerations** **Vish Sundararaman,** Texas Instruments Inc., Dallas **Chair:** Vish Visvanathan, Texas Instruments India
04:00 - 04:15 PM	Break
04:15 - 05:30 PM	**Panel Discussion:** **Participants:** Steffen Rochel, Vish Sundararaman, Nishath Verghese, Atul Sharan, Madhav P. Desai, Vidyasagar Ganesan, Palkesh Jain, Gautam Kapila, Nagaraj N.S. and C.P. Ravikumar **Chair:** Vish Visvanathan, Texas Instruments India

Abstract

Big Challenges for the Semiconductor Industry: Bridging Design and Manufacturing

Juan C. Rey, Mentor Graphics Corporation
Srinivas Mandavilli, Mentor Graphics India

The semiconductor industry is changing at a fast pace when moving to 45 nm and beyond. The long announced DFM (Design for Manufacturability) challenges are reaching a level of consolidation not seen before, as the industry is moving from the independent development of tools and flows to standardization of definitions, and interfaces. This presentation will summarize the CAD tools developed at the interface of design and manufacturing, describe some of the directions being considered to help minimize variability in the physical design and post-tapeout flows, and introduce some of the changes under consideration for 32 nm and beyond.

On-Chip Global Interconnect Using Transmission Line

Kazuya Masu, Tokyo Institute of Technology

On chip global interconnect is usually designed based on RC lumped model and the global interconnect is divided by repeaters to improve the delay time. Because of scaling of metal width/height and ILD spacing, the delay time of global interconnect becomes worse as ITRS has anticipated. Introducing the transmission line concept into global interconnect is a possible candidate to improve the global delay and power consumption. In this lecture, the possible structure of transmission line interconnect with reducing the cross talk, circuits of driver and receiver, circuit performance of transmission line interconnect, comparison of interconnect performance of the transmission line and optical interconnect are discussed.

Interconnect Parasitic RLC and delay Variability below 90nm, Physical Origins and its Impact on the Future Geometry Scaling

Ersed Ackasu, OEA International, Inc.

As the geometries shrink, the statistical variations due to processing starts to play a more significant role in the metal geometry predictability. In addition to that interconnect metal thickness and its width depends on the width printed on the mask as well as on the proximity metal density and its geometry. In the first part of this paper geometry variations due to both of these effects on the parasitic capacitance, resistance, self and mutual inductance and their combined effect on the interconnect delay variability is discussed using three-dimensional extraction techniques. Floating metal effects is also discussed with using appropriate boundary conditions in the Laplace equation for capacitance extraction. In addition to that electrical properties of the interconnect, such as resistivity also becomes width dependent which complicates the problem even more. Assuming that the atom-to-atom spacing is ~5-6 Angstroms, 65nm becomes roughly in the order of 100 atoms wide and this number is shrinking to the order of 50 atoms in finer lithographies! In this case one atom variation in the width will translate to 2% variation. The second part of the paper discusses the effects of the discontinuous nature of the matter on the electrical properties of the interconnect and investigates the bounds of its variability and its resulting discontinuous nature.

Interconnect variability - A front-end perspective

Noel Menezes, Intel Corporation

The lack of correlation in the variations of the metal layers comprising the segments of typical multi-terminal interconnect has led to multi-corner timing analysis being routinely applied. This analysis is primarily carried out to prevent yield problems due to the parametric variations that arise from back-end (interconnect) manufacturing steps. The complexity of analysis at multiple process corners is dominated by the large number of potential corners -- exponential in the number of layers -- caused by interconnect variations. This talk will instead focus on the subtle yet strong interaction between transistor (front-end) and interconnect variations that has not received adequate attention in the design community. Simple, elegant design techniques that can alleviate interconnect variation problems will also be presented.

Thermal Challenges In Integrated Circuit Design

Sachin Sapatnekar, University of Minnesota

As integrated circuit technologies scale, thermal issues are an increasingly important source of uncertainty. Thermally induced effects include short-term changes in the circuit delay and leakage power, as well as accelerated long-term aging that lead to reliability problems. This talk will begin by describing techniques for on-chip thermal analysis in 2D as well as 3D structures. Next, methods that measure the impact of thermal changes on long term and short term performance metrics will be overviewed. Finally, design techniques for recovering from these problems will be presented.

Quality Now Requires - Small Delay Fault Model

Tom Williams, Synopsys Inc

The concept of small delay faults has been discussed for more than 20 years. Methods for determining the relative merits of delay test sets have also been known for 20 years. This was first proposed by Park, Mercer and Williams in 1988. Until recently this area of testing has been considered unnecessary. Today many groups want to use small delay fault testing to achieve high-quality levels. This work will review the derivation of the quality metrics and address how they are used today. Testing for small delay defects requires ATPG-FS[1] tools to understand the design's timing information such that transition delay faults[2] can be detected along longer paths. Timing information is analyzed for use in test automation tools to test for small delay defects. Fundamentals of static timing analysis are analyzed with regard to test. This paper concludes that Signal Integrity[3] information can be ignored by test automation tools when timing information is used to guide ATPG tools towards longer paths. This work also shows that a lack of understanding of clock trees in the long path ATPG algorithm leads to incorrect results.

[1] Automatic Test Pattern Generation (ATPG) is the process of creating a test and Fault Simulation (FS) is the process of determining which modeled failures are detected by tests.
[2] A transition fault represents a lumped-delay-defect (slow to rise or slow to fall) on a given net of the design.
[3] Signal Integrity is used in this paper to mean the impact of capacitive coupling on timing.

Abstract

Process-aware Timing and Power Analysis and Optimization

Steffen Rochel, Blaze DFM Inc.,

Addressing pattern-dependent variability in design using model-based DFM tools

Nishath Verghese and **Atul Sharan**, Cadence Design Systems

As designs migrate to 65nm process technology and below, the impact of systematic manufacturing effects on design functionality and performance is increasing substantially. Manufacturing design layout features of sub-wavelength feature sizes requires a continual increase in the use of optical proximity correction (OPC) and resolution enhancement techniques (RET). Manufacturers today use sophisticated simulation software and model-based methods to perform OPC and RET in mask making. However, designers of chip layout are still using rules (to mimic these models) provided to them by manufacturers - for chip routing, DRC, layout parameter extraction (LPE) and parasitic extraction (RCX). As geometries shrink, the impact of neighboring layout patterns on the printability and electrical characteristics of a drawn shape can no longer be captured effectively using rules. Models of printability and performance impact on transistors and wires due to layout patterns must be made available to designers. "Model-based DFM" tools provide such capabilities to chip designers. Using models calibrated to manufacturing processes, these tools allow designers to predict the systematic impact of pattern-dependent variability on the functionality and performance of their chips. They can be used in conjunction with existing routers, extractors and timing tools to provide insight into the impact of manufacturing effects like lithography, etch, stress and CMP. This talk will focus on methods and tools for model-based analysis and optimization of designs for pattern-dependent variability.

Design-In-Reliability for Interconnect

Nagaraj N.S. Texas Instruments Inc., Dallas, **Palkesh Jain** and **Gautam Kapila**, TI India

The talk walks through the basic concepts of reliability, focusing on the interconnect. As a background, we revisit conventional interconnect reliability guidelines, specifically, electro migration, and related checking procedures. The challenges thrown in to these approaches are highlighted in the light of continued technology scaling and design scaling viewpoint. Power management and statistical process variations are taken as point examples to substantiate the challenges and possible solutions to them are outlined. We also bring in the system reliability perspective and highlight the importance of considering the final application and the complexity of the overall design in the reliability assessment.

Subsequently, we discuss the advances aspects of interplay between interconnect and transistor reliability. Specifically, how the parasitics from interconnects (R, L and C) affect the transistor reliability, namely, gate oxide reliability (TDDB) and negative bias temperature instability (NBTI). On the other hand, the interconnect reliability itself is a function of the transistor age, presenting a case of the joint optimization of the system reliability. The talk eventually motivates designers to move away from traditional sign-off reliability thought process, to a more involved, design-in approach, to achieve higher design and technology entitlement.

On the use of standardized interconnect in VLSI Systems

Madhav P. Desai, IIT Bombay and **Vani Prasad**, Freescale Semiconductors

As VLSI technology scales, wire behaviour tends to become a greater factor in determining the correctness and performance of complex VLSI systems. In order to understand the impact of wire behaviour on the system, it is necessary to accurately model and simulate interconnect in such systems. The accurate modeling and simulation of the interconnect are computationally intensive tasks and often cannot be carried out at early stages in the design flow (such as floorplanning) due to incomplete information. Thus, the system designer often faces the risk of expensive design iterations until she/he achieves design closure. In this talk, we examine the feasibility of using standardized interconnect in the construction of VLSI systems. The advantage of standardization is the availability of pre-characterized and accurate models, which will have an immediate impact on the design closure problem. The potential disadvantages are the possible loss of performance due to standardization and the usability of the standardized interconnect in practical design flows. In this talk we propose a standardized interconnect library consisting only of point-to-point connections. We show that these standardized elements are near delay-optimal (to within two inverter delays of the best possible solution), and further, demonstrate that the bandwidth offered by these elements is superior to that offered by ad-hoc solutions. We also show that complex routes can be constructed from these standard elements using a simple cut-and-splice routing model, which leads to near-optimal routing delays. Further, these conclusions are valid even as technology scales into the deep sub-100nm range. We conclude that standardization of interconnect is feasible and offers a viable solution to the interconnect problem in VLSI system design.

Clocking in GHz designs

Vidyasagar Ganesan, AMD

Variation has always been a part of the semiconductor business. However at sub 100nm the process and environmental variation pose tremendous challenges to designer in meeting the Performance, power and yield targets. In multi GHZ designs, clock distribution needs to have low skew, factoring the variations from device, interconnect and transient conditions. In this talk we will explore clocking schemes, its impact to variations and techniques to minimize them.

Interconnect Design – Packaging Perspectives and Considerations

Vish Sundararaman, Texas Instruments Inc., Dallas

Electronic packaging represents a significant and integral portion of the IC interconnect bridging the silicon device and functionality to the OEM / end-user application. Packaging technologies continue to evolve to keep pace with the ever-increasing complexity and trends in the semiconductor industry towards miniaturization, integration and densification. In this workshop, a general overview of the key packaging capabilities, both existing and emerging, will be introduced. Emphasis will be placed on typical interactions between key post-fab package and assembly processes, materials, design aspects and the overall and intended interconnect design and performance. The content of this workshop will be generic in nature to preserve global impact and perspective while aiming to illustrate the increasingly blurred boundary between silicon and package, and hence highlight the need to include packaging aspects into interconnect design.

About the speakers

Juan C. Rey, Mentor Graphics Corporation

Juan C. Rey is the Senior Engineering Director for the Design to Silicon Division at Mentor Graphics Corporation; his group is responsible for the architecture, design and development of the Calibre line of products used for integrated circuits physical verification and tape out tasks such as design rule checking, layout vs. schematic verification, capacitance, resistance and inductance extraction, resolution enhancement, mask data preparation and design for manufacturing. Juan has 25 years of software development experience ranging from research activities at Stanford University (EE department), to development and management (at Technology Modeling Associates, Cadence and Mentor Graphics) of process and device modeling software. His most recent 15 years have been in Electronics Design Automation and semiconductor processing modeling.

Srinivas Mandavilli, Mentor Graphics India

Dr. Srinivas Mandavilli heads the Hyderabad R&D center of Mentor Graphics India. Mentor Graphics Hyderabad has been in operation for around 10 years and has an employee strength of around 225.

Prior to joining Mentor Graphics, Srini has served in various engineering and management roles at Ionic Microsystems, Motorola, and Hitachi Semiconductor America.. He holds a Ph.D in Computer Science from the Indian Institute of Science, Bangalore, and a B.Tech in Electronics from Indian Institute of Technology, Madras. For his Ph.D thesis in Genetic Algorithms, Srini received the best Thesis award at IISc in 1993, and had over 10 international publications.

Kazuya Masu, Tokyo Institute of Technology

Kazuya Masu received the B.E., M.E. and Ph.D. degrees in Electronics Engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1977, 1979 and 1982, respectively. He was with the Research Institute of Electrical Communication, Tohoku University, Sendai, Japan since 1982. In 2000, he moved to Precision and Intelligence Laboratory, Tokyo Institute of Technology, Yokohama, Japan and he is currently a professor in Integrated Research Institute, Tokyo Institute of Technology. He was a visiting Professor in Georgia Institute of Technology in 2002 and 2005. His current interests are signal integrity and GHz signal propagation in multilevel interconnect of Si ULSI, reconfigurable RF circuit technology, LSI performance evaluation and prediction based on statistical approach, and BEOL process technology.

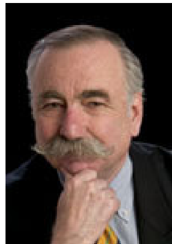
He received IEICE Electronics Society Award in 2005. The paper presented at A-SSCC2006 (IEEE Asian Solid-State Circuit Conference) has awarded as Student Design Contest Outstanding Design Award. He served technical program committee member of international conferences of IEDM (IEEE International Electron Device Meeting), SSDM (International Conference of Solid State Devices and Materials), ADMETA (Advanced Metallization Conference: Japan Session), etc. He is a member of the IEEE, the Japan Society of Applied Physics (JSAP), the Institute of Electronics, Information and Communication Engineers (IEICE), the Institute of Electrical Engineers of Japan (IEEJ), Japan Institute of Electronics Packaging (JIEP), and the Electrochemical Society (ECS).

Ersed Ackasu, OEA International, Inc.

Osman Ersed Akcasu was born in November 3rd 1955 in Istanbul, Turkey. Graduated from Technical University of Istanbul in 1977 with BSEE in Electrical Engineering. In 1980 he received his Ph.D. from University of Bradford, England in Solid State Electronics. His Ph.D. dissertation was "Two Dimensional Mathematical Modeling of Bipolar Transistors". He worked for Harris Semiconductor, Fairchild Semiconductor, Cray Research and Brooktree Corporation, all in the areas of Process and Device Physics and Architecture. Since 1986 his interest was in interconnect related mathematical modeling. In 1988 he founded OEA International, Inc., which is primarily focused on interconnect modeling. He has more than 30 technical articles as first author and several patents.

Noel Menezes, Intel Corporation

Noel Menezes manages Intel's Strategic CAD Labs, which is part of the Design and Technology Solutions division. In the past, he worked on the first automated interconnect design solution applied to Intel's Pentium 4 family of microprocessors. His graduate work on clock tree synthesis and the C-effective delay model for static timing analysis has been applied in the CAD suites of several EDA vendors and VLSI design companies. His current research interests are on techniques to analyze and mitigate the impact of variations in design and advanced cell delay models. Noel holds a B.E. degree from the Maharaja Sayajirao University, Vadodara, and M.S. and Ph.D. degrees from the University of Texas at Austin.



T.W. Williams, Sysnopsys

Dr. Thomas W. Williams is a Synopsys Fellow at Synopsys in Boulder, Colorado, U.S.A. Formerly, he was with IBM Microelectronics Division and manager of the VLSI Design for Testability group. He received a B.S.E.E. from Clarkson University, an M.A. in pure mathematics from the State University of New York at Binghamton, and a Ph.D. in electrical engineering from Colorado State University. He has received numerous best paper awards from the IEEE and ACM, is the founder or co-founder of a number of workshops and conferences dealing with testing, and was twice a Distinguished Visitor lecturer for the IEEE Computer Society.

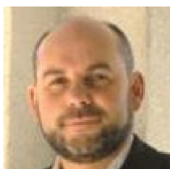
Dr. Williams has previously served on the Computer Society Board of Governors and the IEEE Board of Directors, and was the Society's 2000 Treasurer. He is a member of the Eta Kappa Nu, Tau Beta Pi, IEEE, ACM, Sigma Xi, and Phi Kappa Phi. He is an Adjunct Professor at the University of Calgary, Calgary, Alberta, Canada; and in 1985 and 1997, he was a Guest Professor and Robert Bosch Fellow at the Universitaet of Hannover, Hannover, Germany. He was recently named a member of the Chinese Academy of Science. Dr. Williams was named an IEEE Fellow in 1988 and received the Computer Society's W. Wallace McDowell Award for outstanding contributions to the computer art in 1989. In 2007 Dr. Williams received the European Design and Automation Association Lifetime Achievement Award for "outstanding contributions to the state of the art in electronic design, automation, and testing of electronic systems."

Sachin Sapatnekar, University of Minnesota

Sachin Sapatnekar received the B. Tech. degree from the Indian Institute of Technology, Bombay in 1987, the M. S. degree from Syracuse University in 1989, and the Ph. D. degree from the University of Illinois at Urbana-Champaign in 1992. He has worked at Texas Instruments during the summer of 1990, and at Intel Corporation during the summer of 1997.

He was an Assistant Professor in the Department of Electrical and Computer Engineering at Iowa State University from 1992 to 1997. He is currently a Professor in the Department of Electrical and Computer Engineering at the University of Minnesota, where he holds the Robert and Marjorie Henle chair. His current research interests lie in developing efficient techniques for computer-aided design of integrated circuits, and are primarily centered around physical design, timing and simulation issues, and optimization algorithms. He has authored/coauthored/co-edited five books and has served on the editorial boards of the IEEE Transactions on VLSI Systems (current) and the IEEE Transactions on CAD (currently as deputy editor-in-chief) and the IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing (in the past), has served on the Technical Program Committee for various conferences, including as technical program co-chair for DAC 2006 and 2007. He has been a Distinguished Visitor for the IEEE Computer Society and a Distinguished Lecturer for the IEEE Circuits and Systems Society, and is a recipient of the NSF Career Award, the SRC Technical Excellence Award, and best paper awards at the DAC'97, ICCD'98, DAC'01 and DAC'03 conferences. He is a Fellow of the IEEE.

About the Speakers



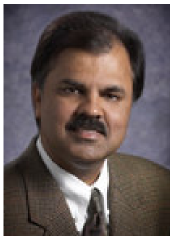
Steffen Rochel, Blaze DFM Inc.,

Dr. Steffen Rochel is the vice president of engineering, Blaze DFM. Dr. Rochel has over 15 years of development and management experience with successful startups and established EDA companies such as Anacad, Mentor Graphics, Simplex Solutions and Cadence. Prior to Blaze, Rochel managed the research and development teams for a number of product lines and technologies at Cadence. He joined Cadence by way of the acquisition of Simplex Solutions where he led the development of the VoltageStorm product line. He has a Ph.D. and Diploma in Electrical Engineering from the Technical University Ilmenau in Germany and has co-authored and presented more than 25 conference papers, journal articles and seminars.

Nishath Verghese, Cadence Design Systems

Nishath Verghese received his BE in Electrical Engineering from BITS, Pilani in 1990, MS and Ph.D in Electrical and Computer Engineering from Carnegie Mellon University, Pittsburgh in 1995. He was a principal at EDA startups Apres Technologies and CadMOS Design Technolology, which was acquired by Cadence Design Systems in April 2001.

From 2001-2004 he was director of timing and signal integrity products in the Digital IC division of Cadence. Subsequently, he was VP, R&D for design products at Clear Shape Technologies, a startup, specializing in model-based DFM analysis software tools. Since Clear Shape's acquisition by Cadence in August 2007, he is serving as group director of electrical DFM and extraction products at Cadence.



Atul Sharan, Cadence Design Systems

Atul Sharan is a 20+ year veteran of the hi-tech industry with experience as an engineer, manager, entrepreneur, senior executive, angel and venture investor. Most recently he was co-founder, President and CEO of Clear Shape Technologies, Inc., which was acquired by Cadence. Prior to Clear Shape, from 1998 to 2003, Mr. Sharan was Senior Vice President, Sales and Marketing for Numerical Technologies, Inc. During his tenure at Numerical, the company grew from pre-revenue stage to a highly successful IPO in April 2000 and was eventually acquired by Synopsys in 2003 where he served as Vice President. Subsequent to that he was resident at Mohr-Davidow Ventures. From 1997 to 1998 Mr. Sharan was in charge of key partnerships and business development at Ambit Design Systems - the company was acquired by Cadence Design Systems in 1998.

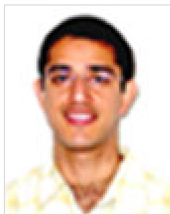
From 1991 to 1997 Mr. Sharan held senior management positions at Compass Design Automation. While at Compass as General-Manager, India Operations, Mr. Sharan helped establish a software development center in India. From 1984 to 1991, Mr. Sharan worked in semiconductor manufacturing operations at VLSI Technologies and Integrated Device Technology. At IDT Mr. Sharan helped initiate the company's first overseas Test and Assembly plant in Penang, Malaysia. Mr. Sharan has an MBA from University of California, Berkeley, an MS in Engineering from Texas and a B. Tech Degree in Engineering from IIT, India. He is a charter member of TIE.

Nagaraj N.S. Texas Instruments Inc., Dallas

Nagaraj NS is the Director of Interconnect Modeling, Design and Performance Closure at Texas Instruments Inc., Dallas, TX. Over the past 17 years, the design methods and solutions developed by him for signal integrity, interconnect modeling, RC extraction, IR-Drop, reliability, variability and DFM in advanced CMOS technologies have been applied on TI's DSP and wireless products. Recently, his work includes defining technology for 45nm and 32nm for ASIC, DSP and wireless products. His research, development and application interests include interconnect modeling, variability, DFM and new architectures for digital and analog products. He has served on Technical Program Committees for DAC, CICC, VLSI Design and ISQED. He received B.E. from UVCE, Bangalore University and Ph.D. degrees from University of Texas at Dallas.

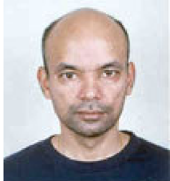
Palkesh Jain, Texas Instruments India

Palkesh Jain graduated from the Indian Institute of Technology (IIT) Bombay in July 2004, with Bachelors and Masters in Electrical Engineering, under the Dual Degree Programme. His Masters research was on Soft Errors. He joined the Reliability CAD Group at Texas Instruments India in July 2004. Since then, he has contributed to the CAD and methodology development for 65nm and 45nm reliability flows, currently leading the CAD efforts for EM and NBTI. His current research interests are in power-performance-reliability tradeoffs and SoC reliability.



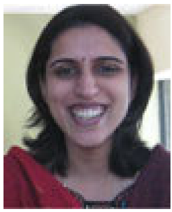
Gautam Kapila, Texas Instruments India

Gautam Kapila obtained his B.E degree from NITK, Surathkal and has been with Texas Instruments for 5 years. He has contributed to Antenna, Channel Hot Carriers, Negative Bias Temperature Instability, Gate Oxide Integrity and Electrostatic Discharge CAD solutions. He contributed to FinFET reliability research, as an assignee at IMEC, Belgium. His main interests are in the areas of reliability CAD solutions, device reliability and technology. He is pursuing a Ph.D. degree in 1/f Noise study in advanced MOS devices from IIT Bombay



Madhav P. Desai, IIT Bombay

Madhav P. Desai received the B.Tech. in Electrical engineering from IIT Bombay in 1984, and the M. S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign. During the period 1992-1996, he worked in the Semiconductor Engineering Group at the Digital Equipment Corporation in Hudson, MA, where he was a Principal Engineer. He is currently an Associate Professor in the Department of Electrical Engineering at IIT Bombay. Dr. Desai's interests are in the areas of VLSI design and design tools, circuits and systems, and combinatorial algorithms. His doctoral work involved the study of the Simulated Annealing algorithm, which is a popular combinatorial optimization technique. While at Digital, Dr. Desai worked on timing verification, delay modeling, circuit and interconnect optimization and contributed to the design of two of the world's fastest CMOS microprocessors. Dr. Desai has been the recipient of GTE and Schlumberger Graduate Fellowships. He has served as a reviewer for the IEEE Transactions on Circuits and Systems, the IEEE Transactions on Computers, the SIAM Journal on Control, and various conferences.



Vani Prasad, Freescale Semiconductor India

Vani Prasad received her PhD degree from IIT Bombay, India. She has been with Freescale Semiconductor, Bangalore, India since 2006, where she is currently a Design Engineer. Her research interests are interconnect design and optimization, physical design CAD and VLSI circuit design issues.

Vish Sundararaman, Texas Instruments Inc., Dallas

Dr. Vish Sundararaman is a Package Engineering Manager at Texas Instruments Incorporated in Dallas, TX, USA. His core responsibilities include packaging readiness to support TI's analog silicon technologies and product portfolios. During his 8 years with TI, his major roles included thermo-mechanical modeling and analytical expertise to support advanced packaging and materials development; he has also made significant contributions to TI's advanced CMOS silicon technologies from development through production. Vish has a B.Tech in Metallurgical Engineering from the Indian Institute of Technology, an MS in Materials Science and Engineering from the University of Notre Dame, and a PhD in Mechanical and Aerospace Engineering from Syracuse University. Vish packaging career began as a Post-Doctoral Research Fellow at the Georgia Institute of Technology's Packaging Research Center.

Vidyasagar Ganesan, AMD

Vidyasagar Ganesan, manages the Soc Design at AMD, India, he has over 14 years experience in the technical management of processor development at Sun Microsystems, Texas Instruments and AMD. Vidyasagar's interests are in technology, clocking, timing and power distribution.

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