

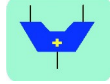


Electronic System Level Design Workshop 2007

January 11 -12, 2007

Venue: **Wipro Learning Center, Electronics City, Bangalore**

Organized by



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THE ARCHITECTURE FOR THE DIGITAL WORLD®

ESLD - 2007, Workshop intent

Raising the level of abstraction to electronic system-level is emerging as a power solution to the problem of design productivity. ESL Design encompasses a number of disciplines, such as system system-level design entry, translation of high-level language descriptions to RTL, hardware-software partitioning, system-level verification, and system-level testing. A number of commercial products and associated methodologies are emerging for ESL Design. The goal of the workshop is bring together a number of practitioners in the area of ESL Design and create a forum for exposing and discussing these methodologies.

Speakers

Prof. Nikil Dutt, UC Irvine
Dr. Rishiyur Nikhil, CTO, Bluespec Inc.
Brian Bailey, Brian Bailey Consulting, USA
Dr. Sachin Ghanekar, Tensilica
Dr. Kanishka Lahiri, NEC-Labs
Dr. Sandeep Shukla, Virginia Tech Univ.
T.S. Rajesh Kumar, Texas Instruments Bangalore
Aravinda Thimmapuram, NXP Semiconductors
Desingh Balasubramanian, Poseidon
Srinivasan Venkataraman, Synopsys
Charlie Hauck, VP Engineering, Bluespec Inc

Organizing Committee

C.P. Ravikumar, Texas Instruments, India
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Alok Kumar, Coware, Noida
Ashish Dixit, Tensilica
A. Vasudevan, Wipro Technologies
Yogendra Rao, Wipro Technologies
N.S. Murty, NXP Semiconductors

Workshop Registration

Before December 25, 2006

After December 25, 2006

	Before December 25, 2006	After December 25, 2006
Professionals (Non-Members)	Rs. 4,000/-	Rs. 4,500/-
Professionals (VSI/ IEEE members)	Rs. 3,000/-	Rs. 3,500/-
Students/ Faculty (Non-members)	Rs. 2,500/-	Rs. 3,000/-
Students/ Faculty (VSI/ IEEE members)	Rs. 2,000/-	Rs. 2,500/-

Please also register using the online registration form at <http://vlsi-india.org/vsi/activities/reg.shtml> apart from sending the filled hardcopy of registration form.

About the Invited Speakers

Nikil Dutt received the BE (Hons) degree from BITS, Pilani, MS from Penn State and PhD from the University of Illinois at Urbana-Champaign, and is currently a Professor of CS and EECS at the University of California, Irvine. His research interests are in embedded systems design automation, computer architecture, optimizing compilers, system specification techniques, and distributed embedded systems. He has received numerous best paper awards and is coauthor of 5 books and over 200 journal and conference publications. Professor Dutt currently serves as Editor-in-Chief of ACM transactions on Design Automation of Electronic Systems (TODAES) and as Associate Editor of ACM Transactions on Embedded Computer Systems (TECS). He was an ACM SIGDA Distinguished Lecturer during 2001-2002, and an IEEE Computer Society Distinguished Visitor for 2003-2005. He has served on the steering, organizing, and program committees of several premier CAD and Embedded System Design conferences and workshops, and serves on the advisory boards of ACM SIGBED and ACM SIGDA.

Rishiyur S. Nikhil is a co-founder and CTO of Bluespec, Inc., which develops a SystemVerilog-based tool that dramatically simplifies and shortens the process of chip design. From 2000 to 2003, he led a team inside Sandburst Corp. developing Bluespec technology and contributing to 10Gb/s network chip designs. From 1991 to 2000 he was at Cambridge Research Laboratory (DEC/Compaq), including over a year as Acting Director. From 1984 to 1991 he was a professor of Computer Science and Engineering at MIT. He has led research teams, published widely, and holds several patents in functional programming, dataflow and multithreaded architectures, parallel processing, compiling, and EDA. He is a member of ACM, IEEE, and IFIP WG 2.8 on Functional Programming. He received his Ph.D. and M.S.E.E. in Computer and Information Sciences from the Univ. of Pennsylvania, and his B.Tech in EE from IIT Kanpur.

Charlie Hauck, who is VP engineering at Bluespec, has more than 25 years experience in research and development, engineering, marketing and management from within the semiconductor industry. Most recently, he was USA General Manager for Faraday Technology, a fabless ASIC vendor and silicon intellectual property (SIP) provider. From 1998-2003, he served as Vice President of Engineering at Lexra Inc., a microprocessor SIP company. From 1994 to 1998, Hauck was director of application specific integrated circuit (ASIC) development at LSI Logic, responsible for advanced ASIC technology and library development. From 1987 to 1994, he was Director of IC Development at Kendall Square Research, managing the very large scale integration (VLSI) design team responsible for delivering working silicon for its custom chips. Hauck began his career at Commodore, where he completed several VLSI chips and boards for consumer electronics and DSP systems.

Hauck holds a BSEE from the Johns Hopkins University and a MSEE from MIT.

ADVANCE PROGRAM AS ON 15-11-2006

Day 1 - Thursday - January 11, 2007

08.00 AM	Registration and breakfast	
09.00 AM	Inauguration	
	Venue - Room Columbus, Wipro Learning Center	
	<p>Session 1-A : Keynote Talk Nikil Dutt, Center for Embedded Computer System, UC Irvine In Search of the Elusive Golden Reference Model for ESLD</p> <p>A critical challenge in Electronic System Level Design (ESLD) is the lack of a golden reference model that can be used across different facets of ESLD, including design specification, HW/SW co-design, co-validation, and downstream CAD flows. Indeed, for the task of validation alone, traditional techniques typically employ different reference models depending on the abstraction level and verification task (e.g., functional simulation or property checking), resulting in potential inconsistencies between these multiple reference models. The problem is further aggravated due to the plethora of different models - generated both automatically and manually - that are used for the tasks of synthesis, simulation, interface generation, estimation, etc. Many open questions remain. How can we manage consistency between these models? Can all of these models be generated from, or linked to a "Golden Reference" model? Is the search for a "Golden Reference" model akin to the search for the proverbial "Goose That Laid the Golden Egg"?</p> <p>This talk will discuss challenges in these domains, and present some possible directions in the context of ESLD for heterogeneous Multiprocessor Systems-on-Chip (MPSOCs).</p>	
10.00 AM	Tea	
10.30 AM	<p>Session-1A Venue - Room Coral, Wipro Learning Center</p> <p>Dr. Sachin Ghanekar, Tensilica Designing a DSP core for audio applications using a Configurable Processor</p>	<p>Session-1B Venue - Room Columbus, Wipro Learning Center</p> <p>Dr. Rishiyur Nikhil, CTO, Bluespec Inc. Design by refinement - An ESL technique that starts from an executable specification and successively refines the design to implementation</p>
11.30 AM	<p>Kanishka Lahiri, NEC-Labs Addressing the Battery Gap: System-level Techniques for Low Power SoC Design</p>	<p>Charlie Hauck, VP Engineering, Bluespec Inc Automated Fine Grain Low Power Design Techniques</p>
12.30 PM	Lunch	
01.30 PM	<p>Session - 1C : Tutorial I Venue - Room Coral, Wipro Learning Center</p> <p>Sandeep Shukla, Virginia Tech University System-level Techniques for Power Optimization</p>	<p>Session -1D : Tutorial II Venue - Room Columbus, Wipro Learning Center</p> <p>Srinivasan Venkataramanan, Synopsys India Improving Verification Productivity using SystemVerilog</p>
03.45 PM	Tea	
04.15 PM	Tutorial Continues	Tutorial Continues
05.30 PM	End of Day 1	

Addressing Battery Gap: System-level Techniques for Low-Power Design

Kanishka Lahiri, NEC Labs

Rapidly escalating energy requirements of the electronics contained within mobile devices are quickly outpacing the capacities of the batteries that power them. There is consensus that this emerging "battery-gap" cannot be effectively addressed through low-level (e.g. circuit-level) techniques alone. This has led to increased emphasis on solutions that can be applied earlier in the design cycle, at higher levels of abstraction (e.g., system-level), when significant opportunities exist for optimizing the application and/or architecture for energy efficiency.

As a step towards bridging this gap, at NEC Laboratories, we have been focusing on developing technologies for analyzing SoC power consumption at the system-level of abstraction. This talk covers an overview of our power analysis framework, which consists of methods to automatically generate IP power models, and techniques for fast and accurate system-level simulation based power analysis. It will highlight new techniques that we use for achieving high power estimation efficiency, namely, hardware acceleration using commercial logic emulation platforms, and adaptive power modeling. A trend that is causing increasing concern is the growing impact of leakage power variations in advanced, sub-90 nm process technologies. It will also describe how our analysis framework effectively incorporates leakage power variations (both die-die variations due to manufacturing, and on-die, dynamic variations due to temperature). And illustrations on the application of such system-level power analysis tools to the design of low-power, battery-operated systems.

TUTORIAL I : SYSTEM LEVEL TECHNIQUES FOR POWER OPTIMIZATION

Sandeep K. Shukla, Virginia Tech

In the changing world of pervasive and ubiquitous computing, extensive use of hand held devices, and biomedical devices, embedded computing is becoming increasingly complex. However, complex functionality must not come at the price of reduced battery life for such devices. As a result, power optimization and low-power design of such devices and systems is extremely important. Power optimization goals can be pursued at various levels of design abstraction, such as gate level, micro-architectural level, architecture level, protocol level, system level and at the embedded software level. In this tutorial, the focus is mostly on system level power management.

Dynamic Power Management (DPM) is one form of system level power management. It entails employing strategies that yield acceptable trade-off between power/energy usage and corresponding performance penalties. These include heuristic shutdown policies, prediction based shutdown policies, multiple voltage scaling and stochastic modeling based policy optimization. DPM strategies got increasingly sophisticated due to improved power manageability of hardware components. In this context, there is a positive feedback in action. Power management techniques show the potential for power savings, and this pushes hardware developers to support more advanced (finer grained and lower overhead) power management modes. In this tutorial, we will provide an over view of the main issues namely, architecture level, and system level techniques of power minimization and management, how they influence each other. However, we will not concentrate on low power VLSI techniques.

The target audience for this tutorial comprises of researchers, graduate students and industrial engineers working in the area of low power design, power management, embedded software and hardware design. No prior knowledge of the field will be assumed, other than understanding of algorithmic methods, system design and standard probability theory, and calculus.

In particular, power management approaches that we will discuss rely on formal techniques for the evaluation of the effectiveness of DPM algorithms. For deterministic models of the system, competitive analysis along with learning techniques provide a reasonable framework for their analysis. Stochastic optimization approaches to DPM can be analyzed using advances in probabilistic model checking techniques.

ADVANCE PROGRAM AS ON 15-11-2006

Day 2 - Friday - January 12, 2007

08.00 AM	Registration and breakfast	
09.00 AM	Session 2A - Keynote Talk The Yin and Yang of Verification Brian Bailey, Poseidon Design Systems Venue - Room Columbus, Wipro Learning Center	
10:00 AM	Tea	
10.30 AM	Session 2B - Launching of System C User Group India Chapter Inauguration by members of System C User Group Venue - Room Columbus, Wipro Learning Center	
11:15 AM	Session-2C : Tutorial III Venue - Room Coral, Wipro Learning Center	Session -2D: Tutorial IV Venue - Room Columbus, Wipro Learning Center
	Tutorial on ESL Design Speaker: TBD	System C Tutorial Desingh Balasubramanian, Poseidon Design Systems
01.30 PM	Lunch	
02.30 PM	Session 2E: ESL in Education Venue - Room Coral, Wipro Learning Center ESL in Education - Panel Discussion Experts from the industry and academia will discuss the topic of including ESL topics in EE/CS curriculum Participants - S. Karthik , Analog Devices, K. Krishna Moorthy , National Semiconductors, S.K. Nandy , Indian Institute of Science. Moderator: Gulur Nagendra , Texas Instruments.	Session 2F : Industrial Practices Venue - Room Columbus, Wipro Learning Center T.S. Rajesh Kumar , Texas Instruments System-level Memory Exploration and Optimization. Aravinda Thimmapuram , Philips Semiconductors. Performance Analysis of Memory Sub-systems Using Virtual Prototype
04.00 PM	Tea	
04.30 PM	Panel Discussion: ESLD in India: Opportunities and challenges Venue - Room Columbus, Wipro Learning Center The panelists will discuss how ESLD may change the landscape of EDA and VLSI Design in India. Moderator: Shiv Tasker , CEO, Bluespec Inc., Panel Members: Ramesh Subbarao , Texas Instruments; Mudit Mathur , Wipro Technologies, Vishal Suresh , NXP Semiconductor; Vinod Malhotra , Poseidon Systems; S.K. Nandy , Indian Institute of Science	
06.00 PM	End of Workshop	

Brian Bailey - Chief Technologist at Poseidon Design Systems

Prior to joining Poseidon, Mr. Bailey was an independent industry and management consultant, having worked with a number of startup companies to help them turn their conceptual ideas into practical realities. Prior to that, he was the Chief Technologist for functional verification at Mentor Graphics.

Brian Bailey is the Chairman of the Accellera Interfaces committee and a renowned industry veteran. He contributed to the introduction of RTL simulation, emulation, mixed abstraction simulation, hardware / software co-simulation and transaction level modeling. During 2005, he published two books on the subjects of design and verification and has published many papers and articles over the past several years. He is actively sought out to appear in panels and conferences.

He has two patents to his name with others pending and is proclaimed to be one of the visionaries in the emerging ESL field. He graduated from Brunel University in England with a 1st class honours degree in Electrical and Electronic Engineering.

