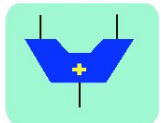


Organized by



<http://vlsi-india.net/>
VLSI Society of India

Electronic System Level Design Workshop 2006

January 9 -10, 2006, Bangalore

**Venue: Golden Jubilee Seminar Hall,
Department of Electrical Communication Engineering
Indian Institute of Science, Bangalore**

In collaboration with
IEEE Circuits and Systems Society
Bangalore Chapter



<http://www.ieee.org>

ESLD - 2006: Workshop Goals

Raising the level of abstraction to electronic system-level is emerging as a power solution to the problem of design productivity. ESL Design encompasses a number of disciplines, such as system system-level design entry, translation of high-level language descriptions to RTL, hardware-software partitioning, system-level verification, and system-level testing. A number of commercial products and associated methodologies are emerging for ESL Design. The goal of the workshop is bring together a number of practitioners in the area of ESL Design and create a forum for exposing and discussing these methodologies.

Speakers:

<p>Prof. Arvind, Massachusetts Institute of Technology, USA Brian Bailey, Brian Bailey Consulting, USA Prof. Rajesh Gupta, University of San Diego, California, USA Dr. Rishiyur Nikhil, CTO, Bluespec Inc. Dr. Shiv Tasker, CEO, Bluespec Inc. Mr. Sarang Shelke, Director Technology, Poseidon Systems, Bangalore Mr. Bill Salefski, VP Technology, Poseidon Systems, California Mr. Viswanath Chakrala, Specialist VLSI System Design, Wipro Technologies, Bangalore</p>	<p>Mr. Sanjay Chakraverty, Senior Manager, IP and Services, Coware, Noida Mr. Himanshu Sanghvi, Project Manager, Tensilica, California Mr Nagendra Gulur Dwarakanath, Texas Instruments, India Mr Badri Gopalan, Ageia, Bangalore Mr Srinivasan Venkataraman, Synopsys, India Mr Raghu Tupuri, General Manager (Silicon Design), Advance Micro Devices, Bangalore</p>
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Day 1: January 9, 2006

08.30 AM	Registration	
09.00 AM	Inauguration	
09:15	Curtain Raiser	
09:30 AM	Keynote 1 - Prof. Arvind, Massachusetts Institute of Technology	How future systems may be designed
10:30 AM	Tea	
11:00 AM	Keynote 2 - Prof. Rajesh Gupta, UCSD	ESL: A Crucial Enabler for Platform Ownership
12:00 NN	Nagendra Gulur Dwarakanath, Texas Instruments, India	System-level Design – Practice and Experience
12:45 PM	Viswanath Chakarala, Specialist, VLSI Systems Design, Wipro Technologies	System C Modeling Approach for SoC Development
01.30 PM	Lunch	
02.30 PM	Sarang Shelke, Director – Technology, Poseidon Design Systems	Processor Based System Performance Acceleration: An ESL Approach
03.15 PM	Sanjay Chakravarti, Sr. Manager, IP and Services, CoWare	
04.00PM	Tea	
04.30 PM	Badri Gopalan, Ageia, India	System Verilog – An Overview
05.30 PM	Srinivasan Venkataraman, Synopsys India	System-level Verification using System Verilog
06.00 PM	End of Day 1	

Day 2: January 10, 2006		
08.30 AM	Registration	
09.00 AM	Keynote 3 - Brian Bailey: ESL? What's that?	
10.00 AM	Tea	
11.00 AM	Keynote 4 - Rishiyur Nikhil, CTO, BlueSpec	A Technical Introduction to ESLD with Bluespec System Verilog
12.30 PM	Raghu Tupuri, AMD	"Systems level design space exploration – Performance Modelling"
01.15 PM	Lunch	
02.15 PM	Himanshu Sanghavi, Project Manager, Tensilica	ESL Requirements for Multiprocessor SoC Design using Configurable Processors
03:00 PM	Tea	
04.00 PM	Panel Discussion: "ESL – Dream or Reality?"	Bill Salefsky, VP – Technology, Poseidon Design Systems
		Shiv Tasker, CEO, BlueSpec
		M. Balakrishnan, IIT Delhi
		Moderator: Brian Bailey
06.00 PM	End of Day 2	

Organizing Committee

C.P. Ravikumar, Texas Instruments, India
 Suhas Hiwale, Poseidon, Bangalore
 Subodh Patil, Poseidon, Bangalore
 S. Jagannathan, Infineon, Bangalore
 Bharadwaj Amruthur, Indian Institute of Science
 Maria Adolf, Bluespec, Germany
 Alok Kumar, Coware, Noida
 Ashish Dixit, Tensilica
 A. Vasudevan, Wipro Technologies

Workshop Registration			
Before December 15, 2005		After December 15, 2005	
Professionals (Non-Members)	Rs. 3,500/-	Professionals (Non-Members)	Rs. 4,500/-
Professionals (VSI/ IEEE members)	Rs. 3,000/-	Professionals (VSI/ IEEE members)	Rs. 4,000/-
Students/ Faculty (Non-members)	Rs. 2,500/-	Students/ Faculty (Non-members)	Rs. 3,500/-
Students/ Faculty (VSI/ IEEE members)	Rs. 2,000/-	Students/ Faculty (VSI/ IEEE members)	Rs. 3,000/-

