Short Tutorials

Paper ID **6** Short Tutorial

Virtual Platform for System Integration and Functional Test
Praveen Kumar* (NXP Semiconductors India Pvt Ltd)

Paper ID **11** Short Tutorial

VMM Methodology Template Code Generator
Lakshman Easwaran*, Vasantha Kumar, Siva Shankar Kuppam, and Ranjith OJ (MindTree Ltd)

Paper ID **42** Short Tutorial

Relevance of Gate Level Simulations in Today's SoC Verification
Vishal Dalal* (SASKEN Communication Technologies Limited)

Paper ID **112** Short Tutorial

A Straetgy and Framework for Processor Verification
Asheesh Shah* (KSU), Ashwani Ramani (DAVV), AbdulAziz Mazyad, and Hamid Elsemary (KSU)

Regular Papers

Paper ID **3** Regular Paper

FPGA based Fuzzy Processing System for Advance Detection of Obstructive and Restrictive Pulmonary Disorders
Shubhajit Roy Chowdhury*, and Hiranmay Saha (Jadavpur University)

Paper ID **4** Regular Paper

An Alternate Approach to Enhance Parallel Decimal Multiplier Performance
Rekha James*, K. Poulose Jacob (CUSAT, Cochi, Kerala), and Sreela Sasi (Gannon University)

Paper ID **8** Regular Paper

High Speed Leading One Bit Detection based New Scaling Free CORDIC Algorithm
Supriya Aggarwal*, Kavita Khare; and Nilay Khare (MANIT)

Paper ID **9** Regular Paper

A Novel Test Method for Fault Detection in RF Circuits
Saravanan P*, Brinda Subburaj, and Kalpana Shekar (PSG College of Technology)

Paper ID **12** Regular Paper

A Novel Low Power and High Read Stability SRAM Cell
Sivamangai N.M, Saravanan P*, and Gunavathi K (PSG College of Technology)

Paper ID **18** Regular Paper

Peak Dynamic Power Estimation of FPGA-mapped Digital Designs
P K Shyamala, Shoaib Mahammad, and Veezhinathan Kamakoti* (IIT Madras)

Paper ID **19** Regular Paper

VLSI Implementation of Motion Vector Recovery Algorithms for H.264 based Video Codecs
Kavish Seth, Muralidhar Komisetty, Vamshi Anand, Veezhinathan Kamakoti*, and S Srinivasan (IIT Madras)

Paper ID **21** Regular Paper

Low-Power Adiabatic Flip-flops and Sequential Circuits using ACPL
Sreenu D*, Ashok Saxena; and Sudeb Dasgupta (IIT Roorkee)

Paper ID **30** Regular Paper

CMOS Analog ASIC Design of Inverse Delayed Function Model of a Neuron for ANN
Niteen Futane, Shubhajit Roy Chowdhury* (Jadavpur University), Chirasree Roychoudhuri (Bengal Engineering and Science University, Shibpur); and Hiranmay Saha (Jadavpur University)

Paper ID **34** Regular Paper

Clock-free Leakage-feedback Gate MTCMOS Flip-flop with a Centralized Sleep switch
Rahul Singh* (IT-BHU, Varanasi)

Paper ID **35** Regular Paper

Addressing Via Density in UDSM Technologies using a Flexible Correct-by-Construction Approach
Dibyendu Goswami*, Swami Gangadharan, and Albert Holguin (Intel)

Regular Papers-2

Paper ID **51** Regular Paper

An Embedded Solution of 2-D Fast Affine Transform for Biomedical Imaging Systems
Pradyut Biswal*, and Swapna Banerjee (IIT Kharagpur)

Paper ID **56** Regular Paper

Mixed-Clock Interconnect FIFO Design
Rakesh Yarlagadda*, Jalapally Karthik, and Hemangee Kapoor (IIT Guwahati)

Paper ID **74** Regular Paper

Prime Numbers are High Coverage Test Vectors!
Vasanthkumar Ramesh, Akanksha Jain, Veezhinathan Kamakoti* (IIT Madras); and Vivekananda Vedula (Intel Semiconductors India)

Paper ID **82** Regular Paper

BIST / Test-Decompressor Design using Combinational Test Spectrum
Nitin Yogi*, and Vishwani Agrawal (Auburn University)

Paper ID **95** Regular Paper

Reduced Verification Effort for Low power SoC by using Right Integration, Simulation and QC Strategy
Mayank Jindal*, Gokulakrishnan Manoharan, Sarveswara Tammali, and Ayon Dey (Texas Instruments India)

Paper ID **100** Regular Paper

Low Power Test Implementation through Temporal Spreading of Scan Shift/Capture and Q-Gating
Pranay Kotasthane*, Sireesha Arisetti, Sreeram Chandrashekar, Kishore Robbi, and Anirban Saha (Texas Instruments India)

Paper ID **104** Regular Paper

Process, Temperature, Voltage (PTV) & Load Compensation for IOs
Vikas Narang* (Texas Instruments), Nitin Chandrachoodan (IIT Madras, Chennai), Vinod Menezes (Texas Instruments)

Paper ID **108** Regular Paper

A 1.8mW, 320MHz Sigma Delta ADC for Wireless Applications
Harish Chandrababu* (IISc Bangalore); and Jamadagni H.S. (CEDT, IISc Bangalore)

Paper ID **110** Regular Paper

Bounds on Defect Level and Fault Coverage in Linear Analog Circuit Testing
Suraj Sindia*, Virendra Singh (IISc, Bangalore); and Vishwani Agrawal (Auburn University, Alabama, USA)

Paper ID **118** Regular Paper

Design of Multiple Output, Field Programmable CMOS Voltage Reference using Floating Gate Transistors
Arsh Josan*, Karan Kumar, and Chota Markan (Dayalbagh Educational Institute, Agra, UP)

Paper ID **120** Regular Paper

Capture Power Reduction for Modular System-on-Chip Test
Jaynarayan Tudu (IISc, Bangalore), Erik Larsson (Linkoping University), Virendra Singh* (IISc, Bangalore), and Adit Singh (Auburn University)

Paper ID **122** Regular Paper

Performance Evaluation of an Efficient Boolean Function Generator for Cryptographic Applications
Debdeep Mukhopadhyay* (IIT Kharagpur), and Ankur Sharma (IIT Madras)

Short Papers

Paper ID **16** Short Paper

A High Performance Reference Circuit using Low Input Offset Operational Amplifier
Anil Saini*, and Kapil Rajput (CEERI)

Paper ID **20** Short Paper

Surface Potential Based Current Modeling of Thin Silicon Channel Double and Tri-Gate SOI FinFETs
Robin Prakash*, Rohit Yadav (BITS, Pilani), and Subhash Bose (Central Electronics Engineering Research Institute, Pilani)

Paper ID **22** Short Paper

Switch Error and Total Harmonic Distortion Improvement Technique in SHA
Rohit Yadav* (BITS,Pilani)

Paper ID **44** Short Paper

Analysis of Single Event Upset for Biomedical Applications
Surendra Rathod, Ashok Saxena, and Sudeb Dasgupta* (IIT Roorkee)

Paper ID **57** Short Paper

Impact of Process Variability on 28nm Analog CMOS Performance
Ajayan R* (IISc, Bangalore)

Paper ID **58** Short Paper

Design and Analysis of Low Power Viterbi Decoder for CDMA System
Ketki Joshi*, Anand Darji, and Upena Dalal (SVNIT,Surat)

Paper ID **61** Short Paper

Performance Evaluation of Mesh-of-Tree Based Network-on-Chip Using Wormhole Router with Poisson Distributed Traffic
Santanu Kundu* (IIT Kharagpur), Radha Dasari (Texas Instruments, Bangalore), Kanchan Manna, and Santanu Chattopadhyay (IIT Kharagpur)

Paper ID **63** Short Paper

Synthesis of Analog Inputs for Testing of Digital Modules in Mixed Signal VLSI Circuits
Chiranjeevi Yarra* (IIT, Kharagpur), Santosh Biswas (IIT, Guwahti), and Siddarth Mukhopadhyay (IIT, Kharagpur)

Paper ID **65** Short Paper

Ultra Low Power Digital to Analog Converter
Raj Dua*, Sumeet Tiwana; and Anu Gupta (BITS-Pilani)

Paper ID **67** Short Paper

Hardware Implementation of Dlighting Module for using it in a Digital Camera Chip
Gaurav Agarwal*, Amit Singhal, Anu Gupta, and Prayush Kumar (BITS Pilani)

Paper ID **69** Short Paper

A Centralized BIST Infrastructure Design for Stuck-At Fault Detection In SoC
Rupsa Chakraborty*, and Dipanwita Roy Chowdhury (IIT Kharagpur)

Paper ID **72** Short Paper

Uniform Thermal Distributions in Placement of Standard Cells and Gate Arrays: Algorithms and Results
Prasun Ghosal, Hafizur Rahaman (Bengal Engineering & Science University); and Partha Dasgupta* (IIM Calcutta)

Short Papers-2

Paper ID **77** Short Paper

Simulation of Improved Dynamic Response in Active Power Factor Correction Converters
Matada Mahesh*, and Anup Kumar Panda (National Institute of Technology)

Paper ID **78** Short Paper

A 1.2-V 5.3–7.3GHz Wideband Quadrature LC Voltage Controlled Oscillator
Mohit Garg, M Sultan M Siddiqui*, and B Bhaumik (IIT Delhi)

Paper ID **83** Short Paper

Design and Implementation of digital baseband modules of CDMA IS-95 and GSM for Reconfigurable SDR
Hari Krishna Boyapati*, Rahul Kumar Misra, Srinivas Gaddam (IIT Roorkee), Somon Raju Kota (CEERI), Ramesh Chandra Joshi, and Karthikeyan Machavaram (IIT Roorkee)

Paper ID **87** Short Paper

Weak Inversion based Low Power Low Noise Sixth order gm-C Filter at 1V for ECG Application with 180nm Technology
Anurag Zope*, Waman Khokle, Raghvendra D. Deshmukh, and Rajendra Patrikar (Visveswaraya National Institute Of Technology)

Paper ID **90** Short Paper

Design of Run Time FPGA Router using JBits 3.0
Hafizur Rahaman* (Bengal Engg. & Sc. Univeristy), Nachiketa Das (Marine Engineering and Research Institute, Kolkata), Pranab Roy (BESUS, Shibpur)

Paper ID **91** Short Paper

A High Performance Implementation of LU Decomposition on FPGA
Manish Kumar Jaiswal*, and Nitin Chandrachoodan (IIT Madras, Chennai)

Paper ID **99** Short Paper

AnAlgorithm for High speed, Low power Implementation of Modular Multiplier
Raju Lampande*, Chandrashekhar Kukade, Raghvendra D Deshmukh, and Rajendra Patrikar (Visveswaraya National Institute Of Technology, Nagpur)

Paper ID **116** Short Paper

EEG-based Driving Fatigue Estimation using Discrete Wavelet Transform
Sangeeta Panigrahy* (KITS, Warangal)

Paper ID **117** Short Paper

Constructing Synthetic Benchmark Circuits to Stress Test FPGAs
L Srivani, Veezhinathan Kamakoti* (IIT Madras), and Ilango Sambasivam (IGCAR, Chennai)