

V DAT2008 - Accepted Papers

Regular Papers

PaperID: 10 Regular Paper	A CMOS Comparator Circuit Optimized for Power-Delay Product and Input-Output Isolation Chetan Parikh* (DA-IICT, Gandhinagar); Amit Gupta (DA-IICT)
PaperID: 15 Regular Paper	Metal Gate CMOS from the Device Variability Perspective H. C. Srinivasaiah* (EPCET); Navakant Bhat (Indian Institute of Science)
PaperID: 18 Regular Paper	Test Pattern Reduction by Simultaneously Pulsing Interaction Clocks Xijiang Lin* (Mentor Graphics Corp); Sudhakar Reddy (University of Iowa); Irith Pomeranz (Purdue University)
PaperID: 32 Regular Paper	On-chip Test Circuits for Fast Interconnects Rajkumar Satkuri* (IIT, Bombay); Marshnil Dave (IIT, Bombay); M. Shojaei Baghini (IIT, Bombay); Dinesh Sharma (IIT, Bombay)
PaperID: 36 Regular Paper	Dynamic Threshold PMOS Switch for Power Gating Naushad Alam* (AMU); Abdul Kadir Kureshi (Aligahr Muslim University); Mohd. Hasan (Aligahr Muslim University)
PaperID: 38 Regular Paper	A Fast and Efficient Crosstalk Closure Methodology for Multi-million Gate SOCs Chirag Gupta* (Texas instrument); Soujanya Sarkar (Texas Instrument); Saravanan Karunavel (Montalvo Systems)
PaperID: 41 Regular Paper	Cellular Automata and LFSR Coupling for Pattern Generation: A Feasibility Study Biplab Sikdar* (Bengal Engg & And Sc Univ); Pushan Mitra (Bengal Engg & Sc University); Prasenjit Ghosh (Bengal Engg & Sc University); Susmit Maity (Bengal Engg. And Science Univ.)
PaperID: 42 Regular Paper	High Speed CML Transmitter with on-chip PVT compensation for improved Gain and Linearity errors Navin Kumar* (IBM India Pvt Ltd); Umesh Shukla (IBM India Pvt Ltd); Sankarareddy Kommareddi (IBM India Pvt Ltd)
PaperID: 46 Regular Paper	Analysis And Comparison of Delay Elements and a New Delay Element Design Sujan Manohar* (Texas Instruments); Pavan Torvi (Texas Instruments)
PaperID: 49 Regular Paper	Mesh-of-Tree Based Network-on-Chip Architecture Using Virtual Channel Based Router Santanu Kundu* (IIT Kharagpur); Santanu Chattopadhyay (IIT Kharagpur)
PaperID: 51 Regular Paper	High Performance Elliptic Curve Crypto-processor for FPGA Platforms Chester Rebeiro (Dept of CSE, IIT Madras); Debdeep Mukhopadhyay* (Dept of CSE, IIT Madras)
PaperID: 64 Regular Paper	Case Studies Towards a Platform Independent Framework for Formal Verification of Hybrid Systems Kusum Lata (CEDT, IISc Bangalore); Jairam Sukumar* (Texas Instruments); Subir Roy (SDTC, TI India); H.S. Jamadagni (CEDT, IISc Bangalore)
PaperID: 82 Regular Paper	March Test for Linked Faults in Random Access Memories Sanjay Thakur* (Texas Instruments)
PaperID: 90 Regular Paper	Functional Verification of Sleep Mode Operation in Low Power Designs at RTL Rudra Mukherjee (Mentor Graphics); Amit Srivastava* (Mentor Graphics); Gargi Mukherji (Mentor Graphics); Abhishek Kesh (Mentor Graphics)

<p>PaperID: 93 Regular Paper</p>	<p>Performance Comparison of CNFET and CMOS Based Full Adders at The 32nm Technology Node Tarun Agrawal* (Aligarh muslim university); Anurag Sawhney (AMU); Abdul Kadir Kureshi (Aligahr Muslim University); Mohd. Hasan (Aligahr Muslim University)</p>
<p>PaperID: 110 Regular Paper</p>	<p>600 MHz 18 Kb Ternary Content Addressable Memory M Sultan M Siddiqui* (IIT Delhi); G S Visweswaran (IIT Delhi)</p>
<p>PaperID: 113 Regular Paper</p>	<p>Ultra Wideband Variable Gain Amplifier Design for Software Defined Radio Applications Neeraj Kumar (IIT Guwahati); Parul Chopra (IIT Guwahati); Roy Paily* (IIT Guwahati)</p>
<p>PaperID: 142 Regular Paper</p>	<p>Analytical Modeling and Simulation of Fixed-Fixed beam RF MEMS Resonator Vaishali Mungurwadi* (BVB College of Engg. & Tech.); Uday Wali (KLE College Belgaum)</p>
<p>PaperID: 150 Regular Paper</p>	<p>A Primal-Dual Solution to Minimal Test Generation Problem Vishwani Agrawal* (Auburn University); Mohammad Shukoor (Auburn University)</p>
<p>PaperID: 161 Regular Paper</p>	<p>Macromodel based Fault simulation of Opamp using Parameters Estimation Kiran Kumar Garje* (IIT Kharagpur); Srikanth Pam (IIT Kharagpur); Amitava Banerjee (IIT Kharagpur); Santosh Biswas (IIT Kharagpur); Siddhartha Mukhopadhyay (IIT Kharagpur)</p>

Short Papers

PaperID: 3 Short Paper	Slew Metric for On-Chip VLSI Interconnect Using Nakagami-M Distribution Rajib Kar* (NIT)
PaperID: 19 Short Paper	A History based Technique for Low Power Bus Encoding Santanu Chattopadhyay* (IIT Kharagpur); Srujan Reddy (IIT Kharagpur)
PaperID: 47 Short Paper	Power Estimation of Different Arbitration Techniques for On-Chip Bus Based Reconfigurable Soc Platform Srinivasan N* (PSG TECH); HemaChitra S (PSG College of Technology); Vanathi P.T (PSG College of Technology)
PaperID: 55 Short Paper	A SEU Tolerant Distributed CLB RAM for In-Circuit Reconfiguration Veezhinathan Kamakoti* (IIT Madras); Karthik Kumar Srivatsa (NIT Trichy); Shyam Venkatesh (NIT Trichy); N. Rama Subramaniam (NIT Trichy); Shoaib Mohammad (NIT Trichy); Noor Mahammad (IIT Madras)
PaperID: 61 Short Paper	Design, Simulation and Testing of a High Performance 15-4 Compressor Shubhajit Roy Chowdhury* (Jadavpur University); Aniruddha Roy (Jadavpur University); Aritra Banerjee (Jadavpur University); Hiranmay Saha (Jadavpur University)
PaperID: 75 Short Paper	Input Assignment Technique for low Power Circuit Testing Subhadip Kundu* (IIT KGP); Kanchan Manna (IIT KGP); Tapas Maiti (College of Engg. & Management, Kolaghat); Santanu Chattopadhyay (IIT Kharagpur)
PaperID: 117 Short Paper	Design of Low Power Low Pass Filter for ECG Application With Deep Submicron Technology Amey Walke* (VNIT, Nagpur); Waman Khokle (VNIT, Nagpur); Rajendra Patrikar (CRL, India)
PaperID: 130 Short Paper	Selecting an Optimum Bias Current for An Auxiliary Amplifier in Gain Boosting Amplifier for Power Optimization Vinayak Pachkawade* (VNIT, Nagpur); Rajendra Patrikar (CRL, India)
PaperID: 133 Short Paper	Slew Rate Improvement Technique for High Frequency and Large Amplitude Signals Benny Thomas* (Indian Institute of Technology); Roy Paily (IIT Guwahati)
PaperID: 134 Short Paper	Low Latency LSB First Bit-Parallel Systolic Multiplier over GF(2^m) Hafizur Rahaman* (BESUS); Prasenjit Ray (); Somsubhra Talapatra ()
PaperID: 162 Short Paper	Containing Switching Activity in Scan Compression Pramod Notiyath* (Synopsys); Tammy Fernandes (Synopsys); Ashok Anbalan (Synopsys); Santosh Kulkarni (Synopsys); Rajesh Uppuluri (Synopsys); Jyothirmoy Saikia (Synopsys); Glenn Boyer (Synopsys); Rohit Kapur (Synopsys Inc); Tom Williams (Synopsys)

Poster Papers

PaperID: 1 Poster Paper	A Framework for Dynamic Analysis of SoC Power Grids at Planning Stage Jairam Sukumar* (Texas Instruments); Jayesh Jayarajan (Delhi College of Engineering)
PaperID: 27 Poster Paper	Design of an RF CMOS LNA using 0.25 micron Technology Pranjal Rastogi (Texas Instruments); Karthik Jayaraman (Analog/ RF Research group, Oregon State University, USA); Rajnish Sharma* (BITS, PILANI)
PaperID: 28 Poster Paper	Performance Comparison of CNFET And CMOS based 8T SRAM Cell in Deep Submicron Abdul Kadir Kureshi (Aligahr Muslim University); Naushad Alam* (Aligahr Muslim University); Mohd. Hasan (Aligahr Muslim University)
PaperID: 35 Poster Paper	Bus Synchroniser technique used in Dynamic frequency Scaling Shalini Sharma* (Freescale)
PaperID: 54 Poster Paper	Leakage-aware Synthesis of Multilevel Logic Circuits based on BDD Manipulation and Output Phase Selection Saurabh Chaudhury* (NIT Silchar); Santanu Chattopadhyay (IIT Kharagpur)
PaperID: 59 Poster Paper	Low Power Discrete time FIR Pulse Shaping Filter Design Algorithm using Linear Programming Technique Shalini Sharma* (Freescale)
PaperID: 67 Poster Paper	Dynamic Profiling in Virtual Prototype Environment Praveen Kumar* (NXP Semiconductors India Pvt L)
PaperID: 71 Poster Paper	Novel Circuits for Two's Complement of a Binary Number Rahul Badghare* (VLSI Design Labs, VNIT, Nagpur); Raghavendra Deshmukh (VLSI Design Labs, VNIT, Nagpur); Rajendra Patrikar (CRL, India)
PaperID: 86 Poster Paper	Optimization of High- Performance RF MEMS Capacitive Shunt Switch for Phase-Shifter Applications at Ku band Avra Kundu* (Jadavpur University); Sasanko Maji (IACS); Bhaskar Gupta (Jadavpur University); Samir Lahiri (); Hiranmay Saha (Jadavpur University)
PaperID: 91 Poster Paper	A Pulse Width modulated DC-DC Buck Converter using On-chip Inductor Rohan Kesireddy (IIT Guwahati); Roy Paily* (IIT Guwahati); Jyothi Bhaskarr Amarnadh (IIT Guwahati); Genemala Haobijam (IIT Guwahati)
PaperID: 144 Poster Paper	Sensor Integration in an RFID Tag for Monitoring Biomedical Signals Sandeep Reddy Munnangi (IIT Guwahati); Roy Paily* (IIT Guwahati); Rakesh Singh Kshetrimaym (IIT Guwahati); Genemala Haobijam (IIT Guwahati); Manikumar Kothamasu (IIT Guwahati)
PaperID: 146 Poster Paper	High-Speed, High-Throughput Pipelined and Parallel Architecture for SPIHT algorithm Anilkumar Nandi* (BVB College of Engg. & Tech)
PaperID: 159 Poster Paper	High Speed Low Voltage Low Power Comparator for Pipelined ADC Meganathan Deivasigamani* (Anna University); Raja Paul Perinbam (Anna University)
PaperID: 164 Poster Paper	HCFG Based Approach for Evaluation of SMP Model for System-on-Chip Communication Ulhas Deshmukh* (Malaviya National Inst. Tech.); Vineet Sahula (MNIT Jaipur)

Embedded Tutorials

PaperID: 37
Tutorial Paper

Cross-talk Mitigation in Coupled VLSI Interconnects

Preeti Sharma (NIT Hamirpur HP); **Gargi Khanna** (NIT Hamirpur HP); **Rajeevan Chandel*** (NIT Hamirpur HP); **Sankar Sarkar** (MITS Rajasthan)

PaperID: 17
Tutorial Paper

Adapting Scan Compression to Designs

Rohit Kapur* (Synopsys Inc); **Anshuman Chandra** (Synopsys Inc.); **Yasunari Kanzawa** (Synopsys Inc); **Tom Williams** (Synopsys)

PaperID: 83
Tutorial Paper

Efficient Modeling of Memory Controllers in SystemC

Aravinda Thimmapuram* (NXP Semiconductors); **Raghunath Gannamaraju** (NXP Semiconductors)

PaperID: 124
Tutorial Paper

Efficient ECO implementation using Logical Equivalence Checking

Sarveswara Tammali* (Texas Instruments); **Mayank Jindal** (Texas Instruments); **Shailesh Ghotgalkar** (Texas Instruments)