VLSI EDUCATION IN INDIA
Obvious Questions: Difficult Answers

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VLSI EDUCATION

- What to teach?
  - Pedagogical considerations
  - Inputs from the industry
  - Need for “domain knowledge”
- How to teach?
  - Commercial tools or Public Domain?
  - Lab and Project Style

VLSI EDUCATION

- How to scale up numbers
  - What is the real need?
  - Ratio of B.Tech. : M.Tech: Ph.D.
  - Faculty training
- How much will it cost
- Where are the resources
  - Industry
  - Government

A Roadmap for Manpower Training in VLSI

"Promoting Microelectronics Education:

The Indian Imperative"

– a review by TCS and IIT Bombay.

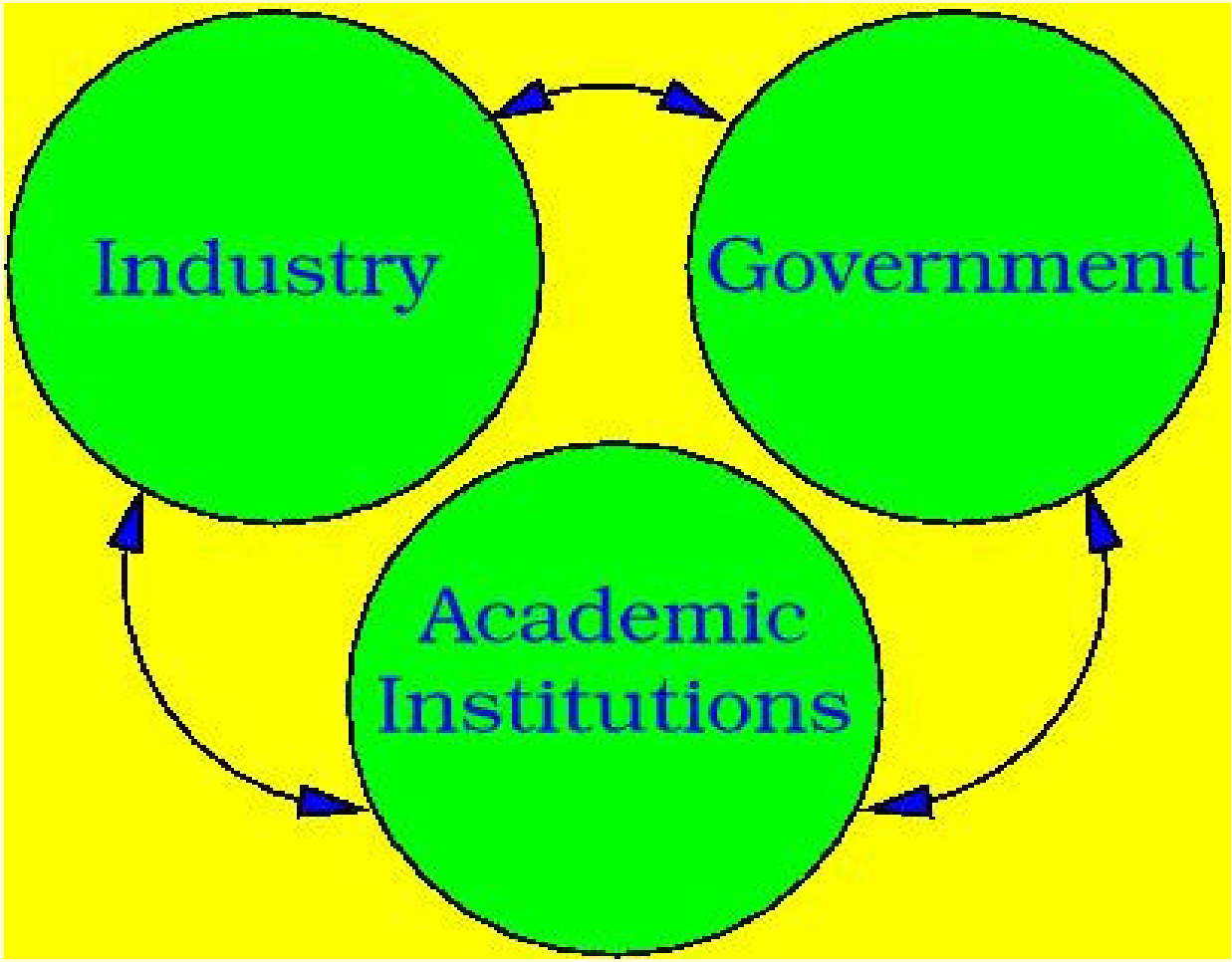
(Informally – the F.C. Kohli report)

4000 to 5000 VLSI Engineers needed per year

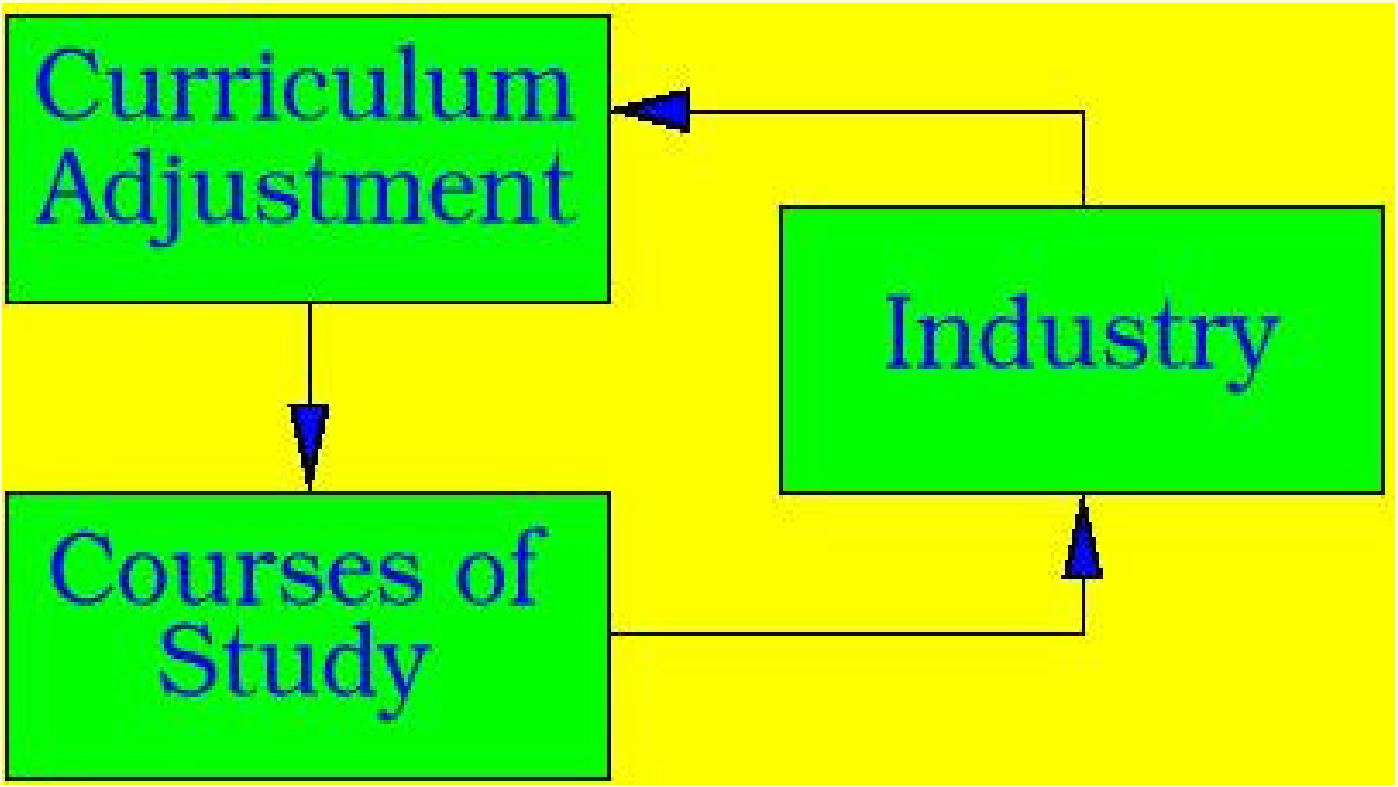
(Current output : About 300 per year)

Special Manpower Development Project of MCIT aims to increase it to about 650 per year.

Partners in VLSI Education



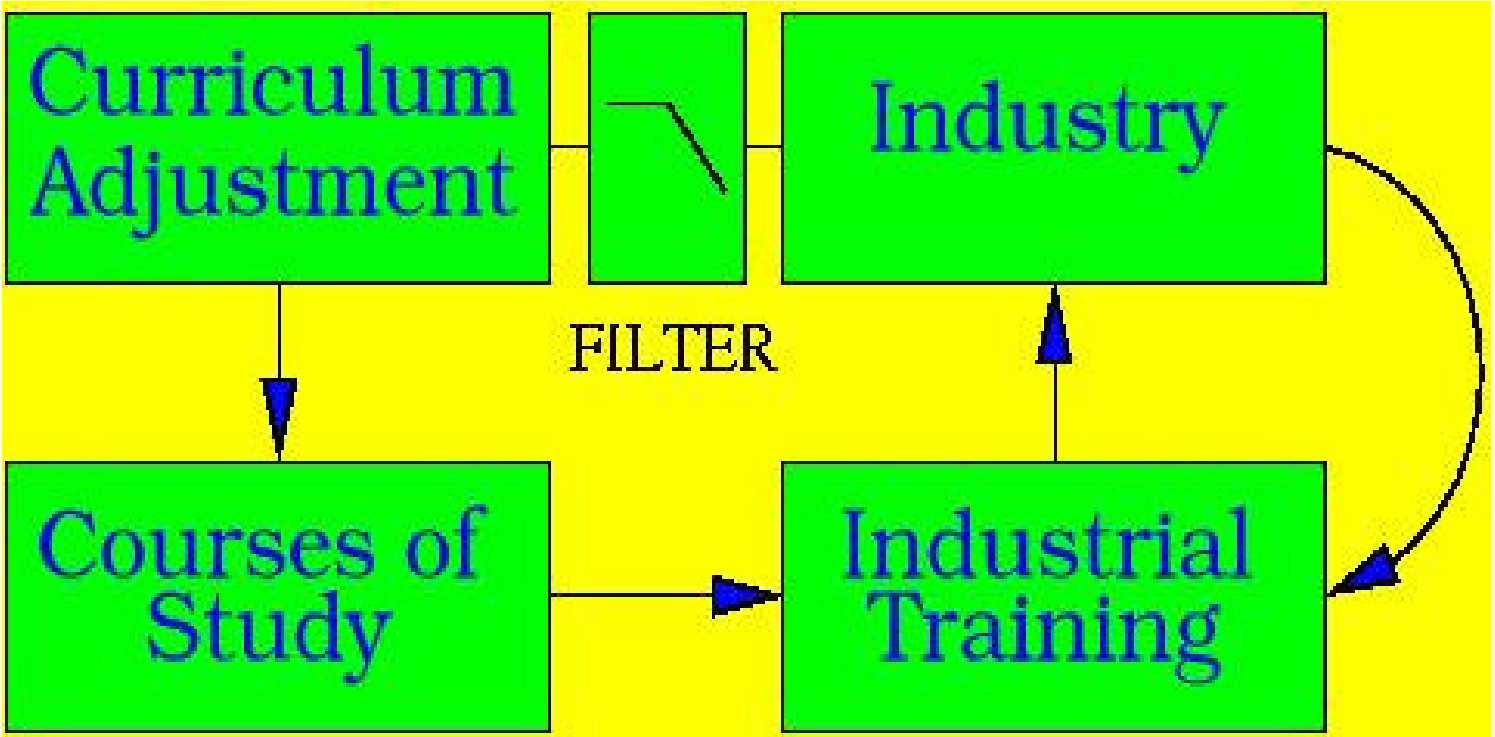
Industry – Academia Interface
Industry Feedback



THE TWO STEP MODEL

- One must distinguish VLSI Education from Industrial training in VLSI Design.
- Different Industries have specific needs for training in the use of some tools or in some narrow areas of VLSI Design.
- These needs are best met through Industrial training – either in-house or through external agencies.

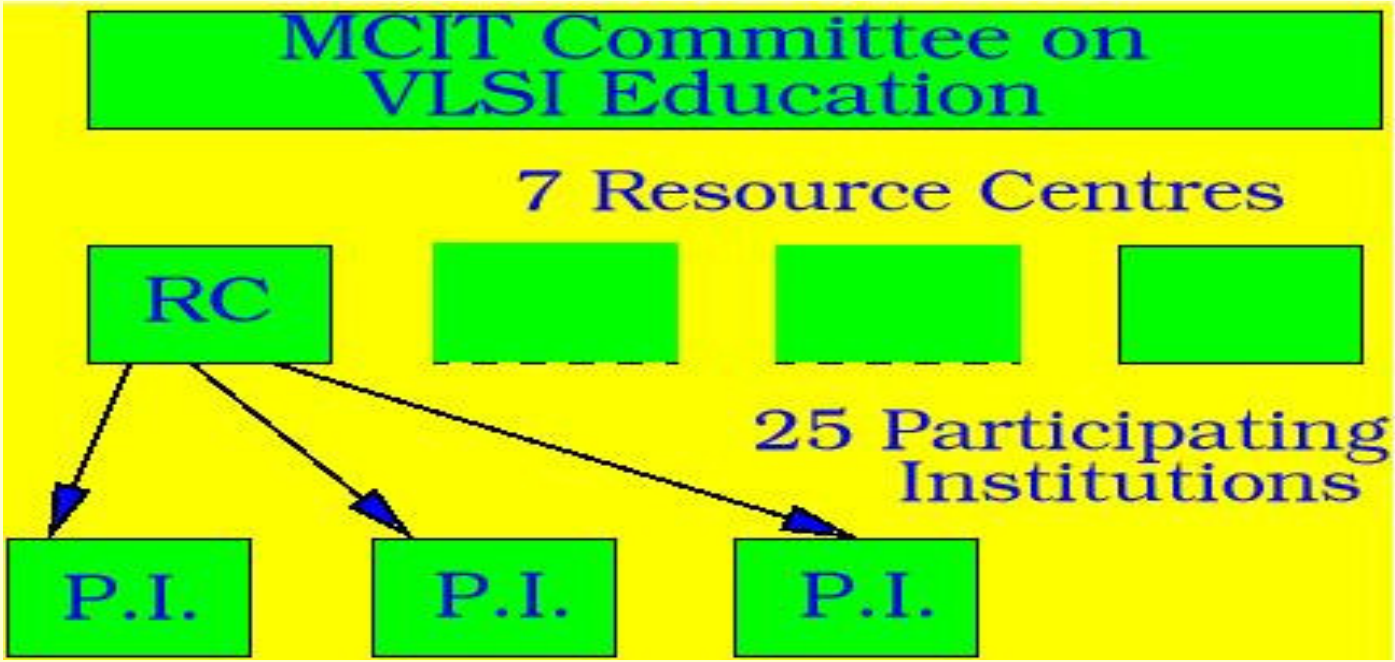
Working with the two step model



Industry Academia Teamwork in VLSI Education

- I.I.T. Delhi with Philips and others
- I.I.T. Bombay with T.C.S.
- I.I.T. Kharagpur – National Semiconductor
- T.I. Academic programmes in DSP
- Intel Laboratories at I.I.T.s, I.I.Sc.
- Faculty training initiative at I.I.T. Bombay (with Intel, IEEE and others)

Special Manpower Development Project of Min. of Communications And Inf. Tech.



OBJECTIVE : To enable a much larger number of institutions in India to produce trained manpower in VLSI and microelectronics

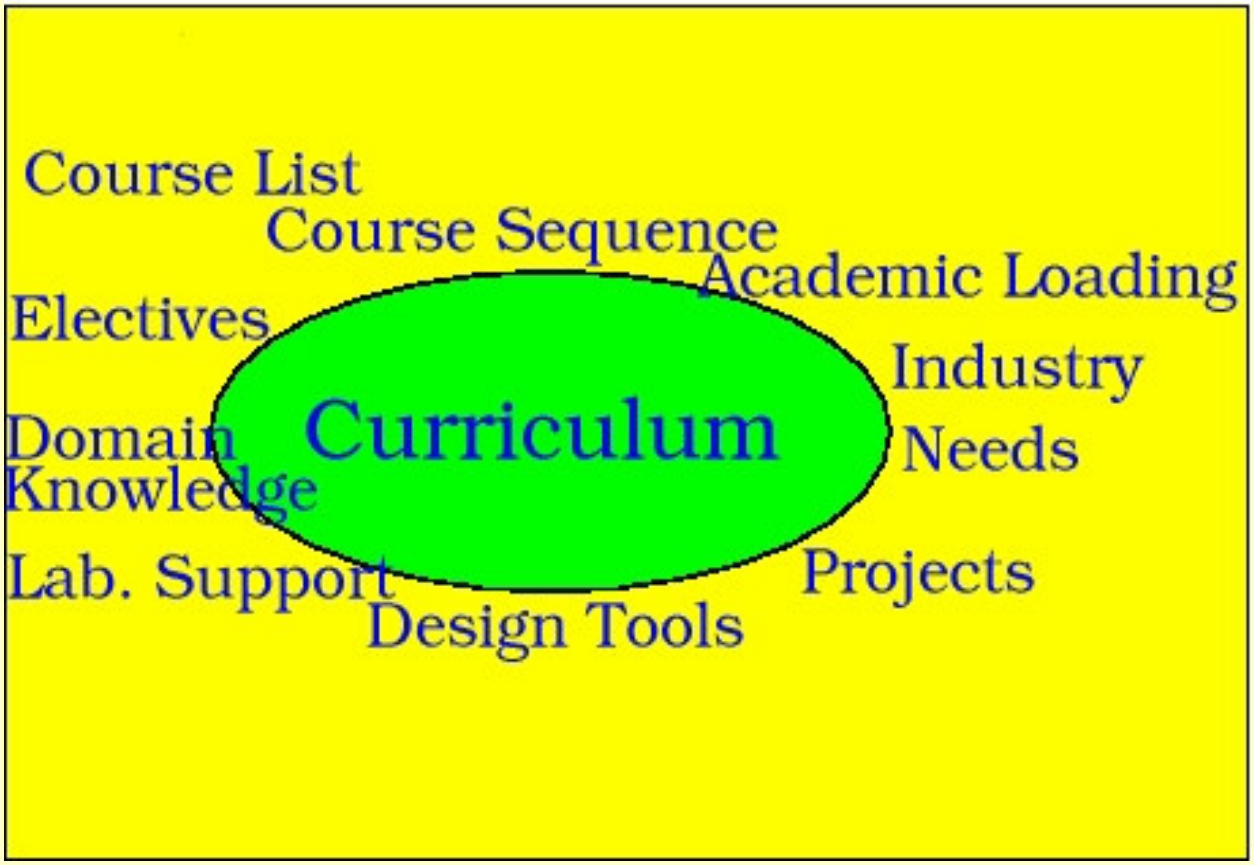
TCS Project on Manpower Development in VLSI

A grant from TCS to IIT Bombay permits admitting twenty additional students to the M.Tech. Programme in microelectronics.

Combined with the original M.Tech. capacity and twenty dual degree students, this brings the number of postgraduate students trained at IIT B in VLSI to above fifty per year.

OBJECTIVE: Development of curriculum and Lab. Structure which can be used at other engineering institutions also.

Designing a Curriculum



M.Tech. (VLSI) course Basic Assumptions

- Specialization through electives
- Academic load of about 40 hrs. per week
  - Assumes each class room hour needs another hour of self study
  - Laboratory courses do not need ‘homework’ time
  - Each course has a load of about 6 hrs/wk – either through 3 lectures or 6 laboratory hours
  - II yr. Devoted to project (+ 1 course)

I Semester

COURSE	Class	Lab.	Home	Tot.
Semiconductor Devices	3		3	6
VLSI Design	3		3	6
VLSI Design Laboratory		6		6
Hardware Descr. Lang.	3		3	6
Elective 1	3		3	6
Technical Comm. Skills	2		2	4
Seminar			4	4

II Semester

Course	Class	Lab	Home	Tot
System Design	3		3	6
Embedded Systems	3		3	6
Test and Verification	3		3	6
Elective II	3		3	6
Project Stage I		16		16

Final Year

Course	Class	Lab	Home	Tot.
III SEMESTER				
Elective III	3		3	6
Project STAGE II		34		34
IV SEMESTER				
Project Stage III		40		40

Elective Courses

Odd Semester	Even Semester
VLSI Technology	Analog Design
Digital Signal Processing	RF Design
CAD for VLSI	Computer Networking
Wireless Comm.	Low Power Design
Device modeling & Sim.	Antennas & Tr Lines

SMDP Curriculum

- I SEMESTER
  - Semiconductor Devices
  - Digital IC Design
  - Hardware Descr. Lang.
  - Electives I and II
  - Tech. Comm. Skills
- III SEMESTER
  - Elective V
  - Project
- II SEMESTER
  - Analog Design
  - Elective III and IV
  - High Level design Lab.
  - Seminar
  - Project
- IV Semester
  - Project

How To Teach

- Laboratory Style
- Choice of Design Tools
- Evaluation Style
- Projects
  - Individual or Team work
  - In house or at Industries
  - Access to Silicon Foundry?

Design Tools

- Public Domain tools
  - Inexpensive!
  - Access to source code
  - Extensible
  - Run on affordable hardware
  - Not so easy to use
  - Not widely used in the Industry
  - May not be accurate enough for taking work to silicon foundry stage

Design Tools

- Professional Tools
  - Expensive!
  - Easy to use
  - Accurate
  - Suitable for Silicon foundry
  - Compatible Libraries available
  - Used in the Industry : hands on experience valuable for students

Suggested Approach

- Use a mix of Public Domain and Proprietary tools
  - PD Tools for instruction
  - Proprietary tools for projects
- Work on developing / improving PD tools
  - Brings Visibility
  - Helps in taking VLSI education to more institutions

Suggested PD Tools

- Spice and ngspice (+ Xcircuit?)
- IRSIM
- Magic
- Icarus verilog / Dynotrace
- GHDL
- Some special purpose tools for synthesis and Petrify etc.

Awareness for PD OS'es like Linux must be increased.

Support Material

- Good text books are now available at reasonable prices
  - Don’t reinvent the wheel
- Teachers’ guides may be required
  - Example problems with solutions
  - Laboratory guides
- Ancillary material
  - Installation guides for Design tools
  - Usage guides for post-processing and visualisation tools

Silicon Foundry

- India Chip programme : SCL
- Access through MOSIS, CMP and Euro-Practice etc. … (Expensive!)
- Is it feasible to have an Indian version of MOSIS?
- Access through the industry
- Test facilities?

Resources

- Cost : about Rs. 3 Lakhs /M.Tech. Student
  - Includes Student support and special labs
  - Does not include costs already incurred by academic institutions such as faculty salaries
- Recurring expense of about Rs. 30 Crores per year for an output of 1000 students/yr.
- Industry MUST contribute in cash and kind.
- Government can provide student support
- Academic Institutes help with faculty time

Expectations from the industry

- Resources
- Student project support
- Access to foundry services
- A representative body of VLSI industries
  - (MAIT etc. are too general)
- Industry-academic forum for sematech like projects

Faculty training

- Instruction Enhancement programmes through SMDP
- Faculty training initiative of I.I.T. Bombay
  - About 10 faculty training courses run per year (In addition to IEP's)
  - Sponsored by IEEE, Industries (Intel)
- Need for distance mode learning

Research

- Ph.D. level training will be increasingly important.
- Facilities at this level are restricted to very few institutions
- Currently, student motivation for Ph.D. is very low.
- Industry consortia should fund and **participate in** research projects.

Conclusions

- This chapter is not over yet!
- Meaningful dialogue between the government, industry and academia required.
- Sharing of responsibilities for VLSI education and training
- Try the current “blue print” and adjust as we go along.